A Low Current High Intercept Point Low Noise Amplifier for 1900 MHz using the ATF-38143 Low Noise PHEMT

Preliminary Applications Information

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Introduction

Hewlett Packard's ATF-38143 is a low noise PHEMT designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. The ATF-38143 has 2 GHz performance guaranteed at a Vce of 2V and Id of 10 mA. The ATF-38143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

The ATF-38143 is described in a low noise amplifier designed specifically for the 1.9 GHz CDMA handset market. PCS applications require a very low noise amplifier coincident with good input intercept point (IIP3). Good input and output return loss improve the cascadability of the amplifier especially when followed by a bandpass filter. The LNA described in this application note has been optimized for a Vds of 2V and Ids of 10 mA although the LNA operates very well at Ids of only 5 mA. At the nominal rated bias, the LNA provides a nominal 0.75 dB noise figure and 15 dB gain. Input and output return loss are better than 10 dB. IIP3 of better than +6 dBm is typical at a supply voltage of 2 V increasing to an IIP3 of +9 to +10 dBm at a supply voltage of 2.7V.

The amplifier is etched on 0.031 inch thickness FR-4 printed circuit board material for low manufacturing costs. The amplifiers make use of low cost miniature wirewound and multilayer chip inductors for small size. The amplifier is designed for a dual polarity power supply whereby the gate voltage can be varied to set the desired amplifier drain current and gain.

Biasing

Passive biasing schemes are generally preferred for their simplicity and resultant low cost. One method of passive biasing requires that the source leads be direct dc grounded. A negative voltage is applied to the gate through a bias de-coupling network. The gate voltage is then adjusted for the desired value of drain current. The gate voltage required to support a desired drain current, Id, is dependent on the device's pinchoff voltage, Vp, and the saturated drain current, Idss. Id is calculated with the following equation.

$$Vgs = (Vp(1-SQRT(Id/Idss)))$$

As an example for the ATF-38143 for a Id of 10 mA, Idss of 118 mA and a Vp of –0.5 volts, the required Vgs is –0.354 volts.

Source Grounding

The inductance associated with DC grounding the device source leads can have a tremendous effect on LNA performance. The use of a controlled amount of source inductance can often be used to enhance LNA performance. Usually only a few tenths of a nanohenry or at most a few nanohenrys of inductance is required. This is effectively equivalent to increasing the source leads by only .050 inch or so. The effect can be easily modeled using one of the HP/EESOF microwave circuit simulators. The amount of source inductance that can be safely added depends on the device. Very short gate width devices such as the 200 micron gate width ATF-36163 can tolerate very little source inductance. Usually the inductance associated with just two plated through holes

through 0.031 inch thickness printed circuit board is all that the device can tolerate. Hence the smaller gate width devices such as the ATF-36163 are typically used as low noise amplifiers for C and Ku Band applications such as TVRO and DBS. The usual side effect of excessive source inductance is very high frequency gain peaking and resultant oscillations. The larger gate widths devices have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be.

LNA Design

The 1X artwork for the generic demo board is shown in Figure 1. The generic demo board gives the designer several design options for both the rf circuitry and biasing options. The demo board is etched on 0.031" thickness FR-4 material for cost considerations.

The designer has the option of using discrete lumped components to minimize layout size or a combination of lumped element and etched microstrip to lower cost. Either low pass or high pass structures can be generated based on system requirements. Low pass matching networks quite often provide an amplifier with the best bandwidth. As a result, the amplifier is more tolerant of component variations. A disadvantage of low pass matching networks is their inability (by design) to roll off low frequency gain. High pass matching networks by design tend to roll-off the low frequency device gain which will minimze the amplifier's susceptibility to low frequency out-of-band interference.
The demo board also allows the FET to be either self biased or with grounded sources the FET can be biased with a negative voltage applied to the gate terminal.

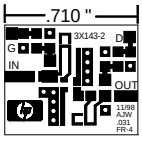

Figure 1 1X Artwork for the ATF-3X143 series of low noise PHEMT devices.

The schematic diagram of the LNA is shown in Figure 2. The amplifier is designed for DC grounded source leads which allows gain to be adjusted by varying the gate voltage Vgg. The parts list is shown in Table 1. The demo board as modified per this application note is shown in Figure 3. The modifications are discussed in the next section.

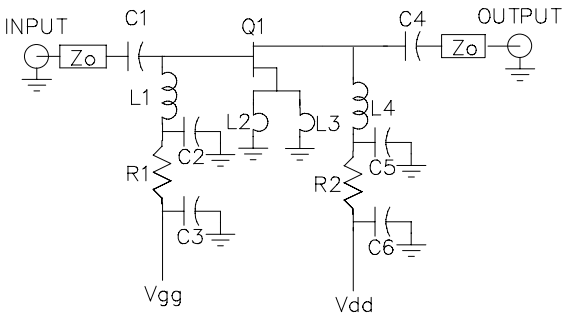

Figure 2 Schematic diagram of the 1.9 GHz ATF-38143 low noise amplifier.

C1	8.2 pF chip capacitor
C2,C5	8.2 pF chip capacitor
C3,C6	10000 pF chip capacitor
C4	3.6 pF chip capacitor
L1	2.7 nH inductor (Toko LL1608-F2N7S)
L2,L3	Strap each source pad to the ground pad with .040" wide etch. The jumpered etch is placed a distance of 0.070" away from the point where each source lead contacts the source pad. Cut off unused source pad. See text
L4	3.9 nH inductor (Toko LL1608-F3N9K)
Q1	Hewlett-Packard ATF-38143 PHEMT
R1	50 Ω chip resistor
R2	12 Ω chip resistor
Zo	50Ω Microstripline

Table 1 Component Parts List for the ATF-38143 Amplifier.

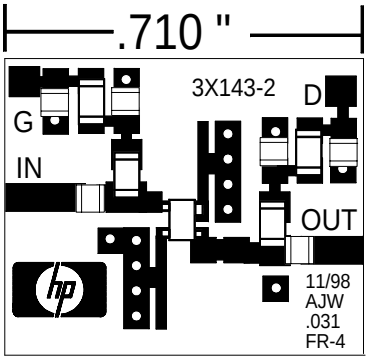

Figure 3 Component Placement Drawing for the ATF-38143 Low Noise Amplifier.

The amplifier uses a high-pass impedance matching network for the noise match. The high-pass network consists of a series capacitor (C1) and a shunt inductor (L1). The high-pass topology is especially well suited for PCS and WLAN applications as if offers good low frequency gain reduction which can minimize the amplifier's susceptibility to cellular and pager transmitter overload. L1 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C2. C1 also doubles as a dc block. The Q of L1 is extremely important from the standpoint of circuit loss which will directly relate to noise figure. The Toko LL1608-F2N7S is a small multilayer chip inductor with a rated Q of 32 at 800 MHz. Lower element Qs may increase circuit noise figure and should be considered carefully. This network has been optimized primarily for noise figure with secondary emphasis on input return loss. Resistor R1 and capacitor C3 provide low frequency stability by providing a resistive termination.

The amplifier uses a similar high-pass structure for the output impedance matching network. L4 and C4 provide the optimum power match for best OIP3 with secondary emphasis on output return loss and gain. L4 also doubles as a means of inserting voltage to the drain. Resistor R2 and capacitor C6 provide a low frequency resistive termination for the device which helps stability. C6 was chosen to be 10000 pF or 0.01 uF over a 1000 pF capacitor in order to improve output intercept point slightly by terminating the F2-F1 difference component of the two test signals used to measure IP3. This can be especially important for the typical 1.25 MHz spacing used in CDMA IP3 evaluation.

The original demo board incorporates additional series microstriplines in both the input and output impedance matching networks. They are not required for this amplifier design and can be removed from the demo board. They should be replaced with a small 0.040" wide piece of etch. There is also space allocated for a resistor in series with the drain of the device. This resistor is also not required for this amplifier design and the gap should be bridged with a small piece of etch.

Inductors L2 and L3 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback . The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstripline which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad would be connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For the 1900 MHz amplifier, each source lead is connected to its' corresponding ground pad at a distance of approximately .070" from the source lead. The .070" is measured from the edge of the source lead to the closest edge of the ground strap. The remaining unused source lead pad should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimize performance. More on this subject next.

Determining the optimum amount of source inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down-side is reduced low frequency gain, however, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone to far?

For an amplifier operating in the 2 GHz frequency range, excessive source inductance will manifest itself in the form of a gain peak in the 6 to 10 GHz frequency range. Normally the high frequency gain roll-off will be gradual and smooth. Adding source inductance begins to add bumps to the once smooth roll-off. The source inductance while having a degenerative effect at low frequencies is having a regenerative effect at higher frequencies. This shows up as a gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some shift in upper frequency performance is OK as long as the amount of source inductance is fixed and has some margin in the design so as to account for S21 variations in the device.

The gain response shown in Figure 4 is for a 2 GHz PHEMT LNA using minimal source inductance. As a result, the amplifier has a fairly smooth gain roll-off at the higher frequencies.

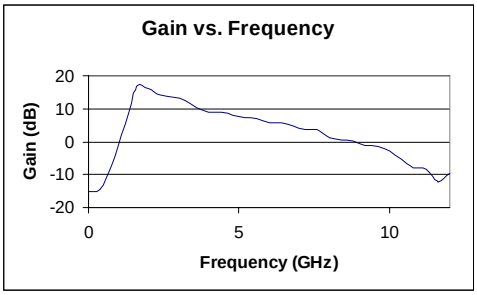

Figure 4 Wide-band gain plot of a 2 GHz amplifier using minimal source inductance.

The gain plot shown in Figure 5 is for the same amplifier that uses additional source inductance to improve low frequency stability and input return loss. Its' effect can be seen as some gain peaking in the 6 GHz frequency range. This level of gain peaking is not considered a problem because of it's relatively low level compared to the in-band gain.

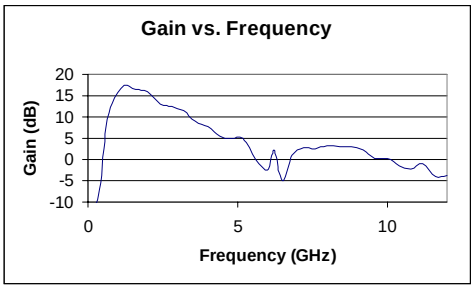

Figure 5 Wide-band gain plot of a 2 GHz amplifier with an acceptable amount of source inductance.

Excessive source inductance will cause gain to peak at the higher frequencies and may even cause the input and output return loss to be positive. Adding excessive source inductance will most likely generate a gain peak at about 6 GHz which could approach 20 to 30 dB. It's effect can be seen in Figure 6. The end result is poor amplifier stability especially when the amplifier is placed in a housing with walls and a cover. Larger gate width devices will be less sensitive to source inductance than the smaller gate width devices. The wide-band gain plot does give the designer a good overall picture as to what to look for when analyzing the effect of excessive source inductance.

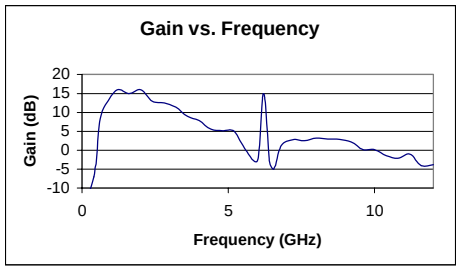

Figure 6 Wide-band gain plot of a 2 GHz amplifier with an unacceptable amount of source inductance producing undesirable gain peaking.

Performance of ATF-38143 Amplifier

The amplifier was characterized at several different bias points. The primary bias point is at a Vds of 2V and Id of either 5 or 10 mA. This requires a power supply voltage of approximately 2.1V maximum. A secondary bias point to be evaluated is at a Vds of 2.6V and 10 mA. This bias point necessitates a power supply voltage of approximately 2.7V while offering several dB improvement in IP3.
The measured noise figure and gain of the completed amplifier is shown in Figures 7 and 8. Noise figure is a nominal 0.7 dB at 1900 MHz at an Ids of 10 mA and at both 2V and 2.7V Vds. Decreasing Ids to 5 mA increases noise figure to about 0.85 dB. Gain at 1900 MHz and a Vds of 2V measures approximately 15.5 dB at both 5 mA and 10 mA Id. Increasing Vds to 2.7V increases gain about 0.3 dB.

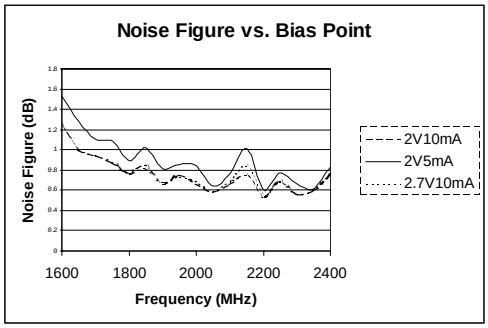

Figure 7 ATF-38143 Amplifier Noise Figure vs. Frequency

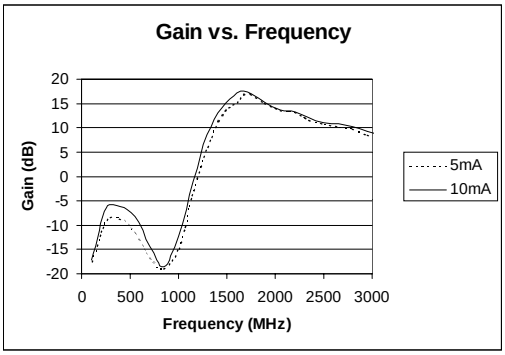

Figure 9 ATF-38143 Amplifier Gain at Id = 5 mA and 10 mA vs. Frequency

The measured input return loss at an Id of 5 and 10 mA is shown in Figure 10. The input return loss at Id = 5 mA measured 13 dB increasing to 14.6 dB as Id is increased to 10 mA. Very little difference in return loss was noted as Vds is increased from 2V to 2.7V.

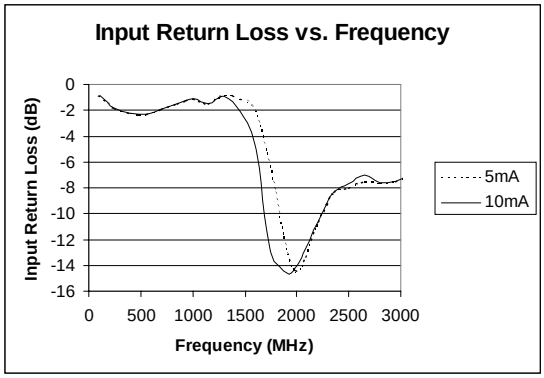

Figure 10 ATF-38143 Amplifier Input Return Loss at Id=5 and 10 mA vs. Frequency

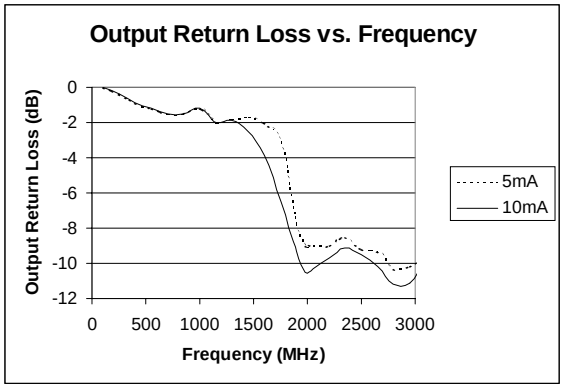

Figure 11 ATF-38143 Amplifier Output Return Loss at Id=5mA and 10 mA vs. Frequency

The measured output return loss is shown in Figure 11. The output return loss measures approximately 8 dB at an Id of 5 mA increasing to 10 dB when increasing Id to 10 mA. The difference in output return loss when varying Vds from 2V to 2.7V is only 0.2 dB.

The amplifier output intercept point (OIP3) was measured at both 1.9 and 2 GHz using two test signals with a spacing of 1.25 MHz. The amplifier input intercept point (IIP3) was then calculated by subtracting the small signal gain. The results of which are shown in Table 2. The OIP3 was measured at a nominal +21 dBm at a dc bias point of 2 volts Vds and an Id of 10 mA. The corresponding input intercept point (IIP3) calculates to be +6.5 dBm at 2 GHz. Increasing Vds from 2V to 2.7V increases OIP3 to +24 dBm at 2 GHz with a corresponding IIP3 of +9.2 dBm.

Bias Point	IIP3(dBm) @ 1.9 GHz	OIP3(dBm) @ 1.9GHz	IIP3(dBm) @ 2GHz	OIP3(dBm) @ 2GHz
2V5mA	+2.5	+18	+4.5	+19
2V10mA	+5.5	+21	+6.5	+21
2.7V5mA	+2.2	+18	+3.7	+18.5
2.7V10mA	+7.2	+23	+9.2	+24

Table 2 Intercept Point vs Bias Point

The ability of the ATF-38143 to withstand a small amount of source inductance has given the designer greater flexibility in obtaining a better input return loss coincident with low noise figure. As a result of using some source inductance, the gain at 2 GHz has been reduced by about a dB from Ga as specified in the data sheet. A side benefit is that input intercept point improves a dB for every dB drop in gain.

Simulation circuit results

The amplifier was designed using the Hewlett-Packard Advanced Design System software. The published data sheet s parameters and noise parameters were first used to perform a linear analysis of the circuit. Gain, noise figure, stability, and input/output return loss are the primary parameters to be evaluated.
It is important to accurately model every component and discontinuity in the circuit in order for any simulation program to yield accurate results. Component parasitics and FET grounding are two areas that without proper modeling can lead to erroneous results. Careful modeling of the gate and drain bias decoupling networks can often assist the designer in providing a stable amplifier especially out-of-band. Figures 12,13,14,15 show the results of the ADS simulation using the published S and Noise parameters at a Vds of 2V and Id of 10 mA. S21, S11 and S22 compare favorably with the measured data. The noise figure compares to within a couple of tenths of a dB at 2

GHz with the only major difference being additional ripple in the measured data. This is probably due to VSWR interaction between the noise source and device under test. The stability factor plot shown in Figure 15 shows that K is near 1 at 2 GHz and significantly better than 1 at all higher frequencies. The stability at 2 GHz can be improved by using a resistor in series with the drain or a slight amount of additional source inductance. Be careful not to add excessive source inductance as stability will get worse at higher frequencies. Simulating S11, S22, and S12 at higher frequencies is also a good idea to help prevent any potential gain peaking which could create stability problems.

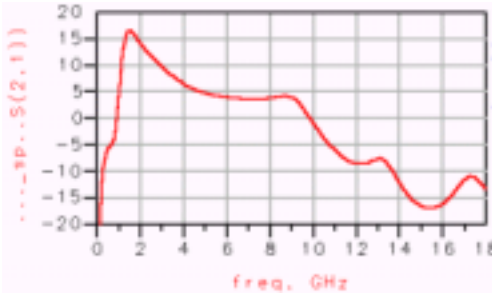

Figure 12. HP ADS Simulation showing S21

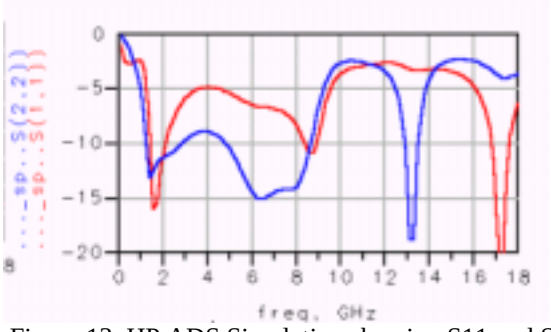

Figure 13. HP ADS Simulation showing S11 and S22

Figure 14 HP ADS Simulation showing Noise Figure

Once a good linear analysis has been performed using the published S and Noise parameters, the non-linear model for the FET can be substituted into the circuit. In the case of the ATF-38143, Hewlett-Packard supplies the Statz model for the die and the associated package model. Using the published Statz and package models, ADS predicts OIP3 values very similar to those presented in table 2.

.**Conclusion**

A high dynamic range LNA has been described using the Hewlett-Packard ATF-38143 low noise PHEMT. At 10 mA drain current, the ATF-38143 provides a very low sub 1 dB noise figure along with high input intercept point making it ideal for PCS and other applications. In addition to providing a low noise figure, the ATF-38143 can be simultaneously matched for very good input and output return loss, making it easily cascadable with other amplifiers and filters with minimal effect on system pass-band gain ripple. It has also been shown that with the published S and Noise parameters, HP Ads predicts comparable performance to that measured on the bench. The Statz non-linear model can also be used to predict non-linear performance with reasonable accuracy.

A.J. Ward September 15, 1999

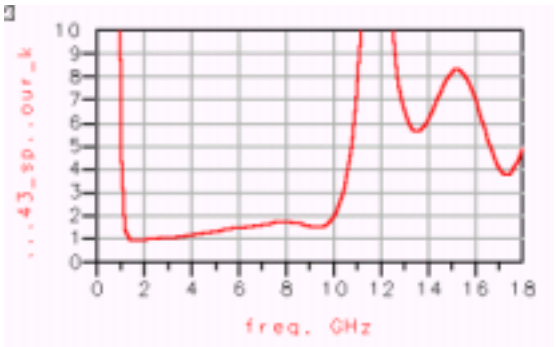

Figure 15. HP ADS Simulation showing Stability Factor K