PH9 Reliability

Application Note # 51 - Rev. A

MWTC MARKETING
March 1997

1.0. Introduction

This application note provides a summary of reliability and environmental testing performed to date on 0.25 µm gate length PHEMT processes (PH9A and PH9B) at HP-MWTC. The information provided is typical of devices from the PH9A and PH9B processes and is meant to supplement PH9 MMIC data sheets.

Included in this application note are descriptions of the reliability experiments performed and the test results for the following topics:

- Thermal Resistance
- HTOL Testing
- ESD Sensitivity
- Bond Pull
- Circuit Level Reliability

2.0. Thermal Resistance

High Temperature Operating Life (HTOL) tests are standard tests used to determine the reliability of active and passive devices from a semiconductor process. The accuracy of HTOL tests depends strongly on operating the devices being stressed at known elevated temperatures. Thermal resistance is the important parameter which is used to set these elevated device temperatures. Thermal resistance is the temperature gradient from the active region of a device to the backside, or the mounting surface of the device, and has units of degrees per watt. The thermal resistance of a device is not a constant but varies depending on geometry, power dissipation and the backside temperature. Active and passive devices from the PH9 process have been extensively characterized to determine their thermal resistances at the HTOL stress temperatures.

Physical measurements of a FET's channel temperature under operating conditions are not possible. Liquid crystal measurements, if carefully performed, provide an averaged temperature of the gate area of the device which is approximately equal to the channel temperature. The average is over a region within about a micron from the hottest spot. However, because of this averaging, liquid crystal measurements generally underestimate the hotspot temperature of the active channel. A thermal modeling program has been developed from the extensive thermal testing done on process monitoring devices in the PH9 process. The short gate length of the PHEMT process makes thermal characterization very tedious and difficult. Careful studies using liquid crystal thermography and other thermal measurement capabilities have provided the physical data necessary to develop the thermal models and accurately determine the device operating temperature. The models can be scaled for different size devices which is necessary to provide thermal analysis of MMICs. The accuracy of these models has been verified and the results correlated to the process monitor FETs used in the HTOL test program described in the next section.

3.0. High Temperature Operating Life (HTOL)

During the process development and qualification stages, HTOL is performed on many wafers. In production phase, an HTOL auditing program is instituted where samples from several random wafers are tested each month.

3.1. Active Device (FET) HTOL Testing

The active devices used for HTOL testing are PHEMT 240 µm FETs which are generally located in the test chip of each reticle. The typical characteristics of these FETs is given in Table 1.

Table 1: PHEMT Characteristics

Total Gate Width	240 µm
Number of Gate Fingers	8
Gate-to-Gate Spacing	15 µm
Gate Length	0.25 µm
I_{DSS} (V_{DS} = 5V)	440 mA/mm
BV_{GDO} (I_G=1 mA/mm)	12V
G_M (peak)	370 mS/mm
Thermal Resistance[1]	330°C/W

1. Measured at T_A = 225°C, P_D = 225 mW; includes the thermal resistance of the 24 pin package.

Samples from each wafer are solder die attached to a molybdenum pedestal. The pedestal is epoxied to the floor of a 24 pin gold-plated package using Ablebond 71-1; there are nine devices per package. The packages are installed into a reliability testing fixture and the devices are biased at a drain current of 188 mA/mm. The packages are then heated until the FET channel temperature reaches the desired aging temperature, usually 275°C or greater. Periodically, the devices are removed from the heat and a variety of operational parameters are measured until failures are noted. Failures at each temperature are recorded until the log normal distribution can be plotted and the activation energy determined using the Arrhenius relationship:

$$\text{lifetime} \sim e^{\left[\frac{Ea}{kT}\right]}$$

For GaAs FET devices, G_m and I_{dss} are normally the first parameters to fail. Failure for G_m and I_{dss} is defined as a 10% drift of the measured parameter.

In the PH9 process, three significant HTOL studies have been performed at 275°C, 300°C and 325°C. Conditions of these studies are described in Table 2.

Table 2: Conditions of PH9 HTOL Program at Three Temperatures

	Channel Temp.		
	275°C	300°C	375°C
Number of Devices	40	417	75
Number of Wafers	6	48	9
Drain Voltage (V_{DS})	5	5	5
Drain Current (I_{DS})	45	45	45

Table 3 presents the failure rate and MTTF extrapolated to 150°C. The reliability goal for MMICs operating at the maximum temperature is that all parameters project a MTTF $> 10^6$ hours and a failure rate less than 200 FITs in one year.

Table 3: Reliability Results at Three Temperatures

	I_{DSS}	G_M
Activation Energy (Ea)	1.62 eV	1.62 eV
Failure Rate in 1 year @ T_{ch} = 150°C	<<1 FIT	<<1 FIT
Median Time to Failure (MTTF) @ T_{ch} = 150°C	3.1 x 10^7 hrs.	5.2 x 10^7hrs.
Shape Factor, Sigma	1.1	1.3

Figures 1 and 2 show the log normal distribution of failures for I_{dss} and G_m. Figures 3 and 4 present the Arrhenius plots for I_{dss} and G_m.

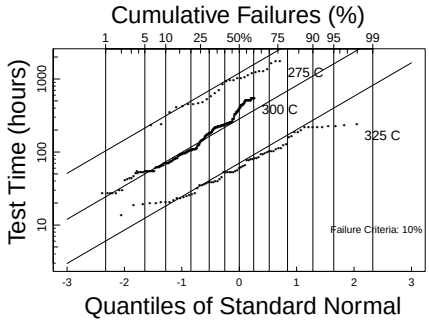

Figure 1. Log-Normal Distribution of I_{DSS} Drift Failures

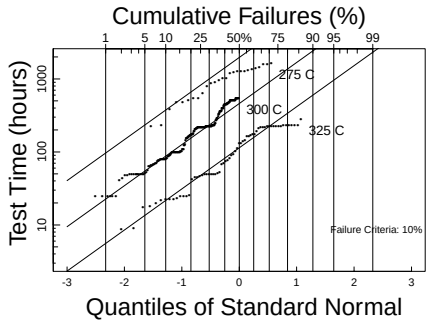

Figure 2. Log-Normal Distribution of G_M Drift Failures

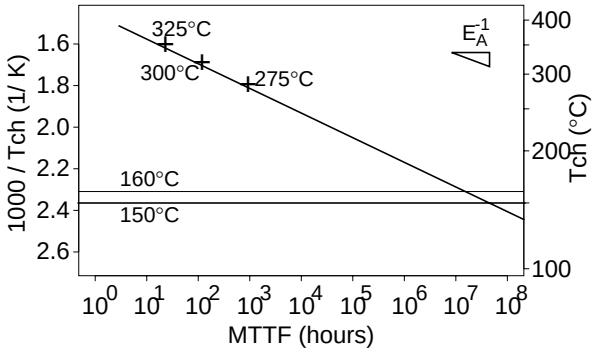

Figure 3. Arrhenius Plot for I_{DSS}

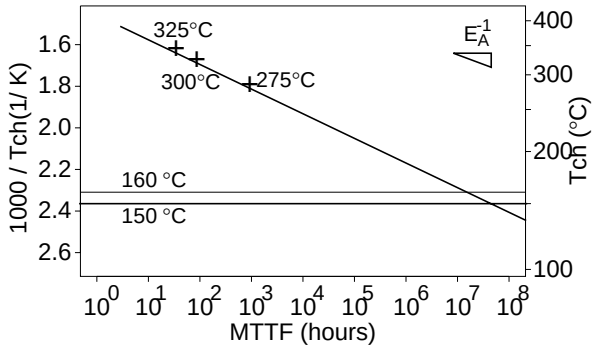

Figure 4. Arrhenius Plot for G_M

3.2. Passive Devices

In addition to the active device HTOL program, HTOL testing is performed on passive devices that may affect MMIC operation lifetime. HTOL testing of passive devices requires understanding of the dominant wearout mechanism for each, and how to accelerate it. Most of the passive devices used in the PH9 process are fabricated using the same process steps as other production MMIC processes at HP-MWTC. Results from reliability testing of these devices in the other production processes are used for inferring the corresponding PH9 reliability.

3.2.1. Resistors

Tantalum nitride resistors are thin film devices where the resistance material is deposited on the substrate surface. The temperature coefficient of TaN resistors is ~200 PPM/°C. They are usable from a few ohms to several hundred ohms. Recommended power dissipations is less than 0.1 mW/μm^2.

Thin film tantalum nitride resistors were HTOL stressed at 0.1 mW/μm^2 and 0.2 mW/μm^2 at 175°C for 2000 hours. At 0.2 mW/μm^2 and T_{amp} = 175°C, the resistor temperature is estimated to be 306°C. The results are summarized in Table 4. These tests were performed in the MMICB process.

Table 4: Resistor Reliability

Type	Stress W/μm^2	# of Devices	% Drift 2000 Hrs.
Ta_2N	0.1	40	1.25
Ta_2N	0.2	<10	4.38

3.2.2. Capacitors

The capacitor is a MIM capacitor with Silicon Nitride and has a 1000Å thickness.

Over 2500 25 pF Silicon Nitride capacitors have been subjected to timed ramp breakdown voltage stress. Analysis of the data and acceleration factors indicate that only about 0.15% of the 25 pF capacitors are projected to fail in less than one million hours at 10V and 150°C.

4.0. ESD Sensitivity

GaAs MMICs are ESD sensitive. As a result, unprotected PH9 FETs are damaged by ESD voltages as low as 200V; however, these same FETs in a circuit may not be damaged by voltages many times that. Proper precautions should be used when handling these devices. (See section 6.6)

5.0. Bond Pull Results

Bond pad adhesion tests are performed using a West Bend bond pull machine. A 0.7 MIL wire is bonded to the PH9 circuit using the standard recommended bonding procedures. The other

end of the wire is bonded to the substrate to which the chip is die attached. The wire bond is pulled from the middle until the bond pad adhesion or the wire fails. The force required to cause failure is measured.

All HP-MWTC processes are tested for bond adhesion. To date >30 wafers from PH9 process have been tested. The minimum pull force and the standard deviation is 3.0 gm and 0.5 gm, respectively. In all cases the wire failed, and not the bond pad.

6.0. Circuit Level Reliability

Circuit level reliability results for selected circuits from MWTC's PH9 process are summarized in this section.

6.1. HMMC-5040 20 - 40 GHz Amplifier

The HMMC-5040 is designed in the PH9B process, which differs from the PH9A process in its power handling capability. The PH9B process allows larger peak swings in the RF voltage and thus higher RF power. The maximum voltage swing allowable between drain and gate is a complex function involving increased gate leakage currents, increased harmonic content, and the potential for gradual output power degradation. The PH9B process provides an extra margin of safe operation at higher power levels than the PH9A process, which has better low noise performance and a slightly higher f_t.

A separate application note covering the HMMC-5040 reliability testing is available (AN#46).

6.2. HMMC-5040 RF Stress

HMMC-5040 amplifiers have been subjected to excessive RF power on the input to determine the catastrophic failure level for the amplifier. After burnout, the circuit is analyzed to determine the failure mechanism. The HMMC-5040 will withstand up to 27 dBm on the input. The failure mechanism is the 50 ohm input matching resistor. Note: While the circuit may withstand these high RF levels for short periods without burnout, continuous operation beyond the safe operating region may result in reduced reliability and gradual output power drift.

6.3. HMMC-5618 HTOL Testing

This amplifier is an efficient two-stage 5.9 GHz to 20 GHz cascadable gain block. The amplifier operates from a single 5V, 115 mA supply. Fabricated in the power robust PH9B process, the amplifier features 14 dB gain with P_{out} = 18 dBm at P_{-1}; 20 dBm P_{sat}.

Amplifiers from three wafers (four to eight devices per wafer) were assembled and tested for HTOL. The devices were biased with a single 5V supply. The devices were heated until the channel temperature was 300°C. Periodically the devices were removed from the heated environment and tested. DC parameters, S-parameters, and power performance were measured. There were no catastrophic failures in 508 hours of HTOL testing; additionally, none of the amplifiers drifted out of spec. A failure criteria was assumed for purpose of developing an Arrhenius analysis of the circuit; S_{21} drift of 0.1 dB provides an MTTF greater than 4 million hours (>100 years). The activation energy from the process monitor FET testing was used for this HMMC-5618 HTOL test.

6.4. HMMC-5023 HTOL Testing

The HMMC-5023 is a four stage LNA in the PH9A process. The amplifier, when operated at the maximum recommended bias level, is well below the 200 mA/mm stress level used to qualify the process. The MTTF and failure rate for the HMMC-5023 were calculated from the PH9A FET reliability data. This calculation projected a MTTF greater than 40 million hours for HMMC-5023 operating at a backside temperature of 125°C. The failure rate in FITs is 0.2 at one year.

6.5. HMMC-5023 Step Stress

Step stress tests on eight packaged HMMC-5023 circuits were performed. The FET channel temperature was increased from 200°C to 300°C in 25° steps. Each temperature was applied for 40 to 96 hours. These tests were used to determine the NF reliability and to note drain current and gain decreases. From these tests the NF increased 0.27 to 0.89 dB (a 1 dB change was the failure criteria [FC]); 3.2% to 9.6% decrease in I_d (10% FC); and a decrease in gain of 0.6 to 4.0 dB (4.0 dB is FC). From these tests the MTTF at 150°C extrapolates to greater than one million hours.

6.6. HMMC-5023 ESD Stress Tests

HMMC-5023 circuits were subjected to ESD tests. Each of the three terminals were subjected to both polarities of ESD voltages in 50 volt increments until failures were measured. The input terminal has a shunt inductor to ground which provides ESD protection. The input terminal withstood 2300 volts. The RF output terminal failed at 250 to 400 volts, and the bias terminal failed at +150 and –250 volts. Careful handling with approved ESD protection is required when handling MMIC chips.

6.7. HMMC-5023 RF Stress Tests

HMMC-5023 circuits were subjected to an RF step stress applied to the RF input terminal. No degradation in performance was measured after ten minutes of exposure at the maximum of 25 dBm. With 25 dBm on the input, the LNA was in severe compression with only 10 dBm on the output. This is far above normal LNA operation and the maximum input specification is set at 15 dBm. Note: Continuous operation beyond compression is not recommended and may result in reduced reliability or output power drift.

For additional information please contact your local HP sales office.