HMMC-1002 ATTENUATOR: ATTENUATION CONTROL

Application Note # 37 — Rev. B

MWTC MARKETING
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I. Introduction

The HMMC-1002 is a voltage variable attenuator that operates from DC to 50 GHz. This application note highlights the advantages of the HMMC-1002 topology versus those of more traditional attenuators and explains the function of the DC reference circuit located on the HMMC-1002 chip. An example of a driver circuit for the attenuator is presented. Advantages and disadvantages of the given driver circuit are also discussed.

II. Topology

A schematic drawing of the HMMC-1002 attenuator is shown in Figure 1. Traditional GaAs FET attenuators are based upon the standard resistive T- configuration using FETs as the series and shunt resistors. This topology is practical for low-frequency applications; however, at microwave frequencies, the parasitic and solid state capacitances of the FETs degrade the performance of T-attenuators.

The distributed topology of the HMMC-1002 increases the operating bandwidth of the device by compensating for the FET capacitances. Instead of using one shunt FET, the HMMC-1002 has four shunt FETs separated by high-impedance, inductive transmission lines. At minimum attenuation, the shunt FETs are essentially capacitive and combine with the inductive lines to form a lumped-element, 50-ohm transmission line. This reduces the high-frequency roll-off of the device in its minimum attenuation state. At maximum attenuation, the high-impedance lines combine

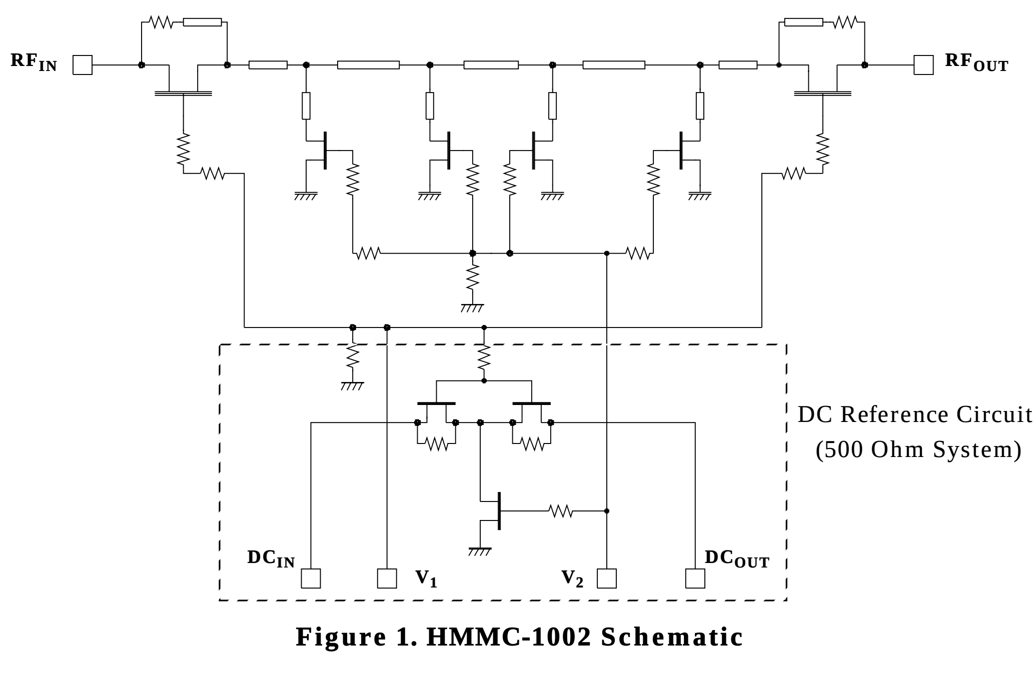

Figure 1. HMMC-1002 Schematic

with the low resistance shunt FETs to form series-L, shunt-R, low-pass filters. This four-section filter rejects high-frequency signals that leak through the series FET capacitors. The net result is an attenuator with a dynamic range of 38 dB at 26.5 GHz. (Note: Due to the low-pass filter structure inherent in the distributed design, the dynamic range is greater at high frequencies than it is as low frequencies.)

III. DC Reference Circuit

A. Operation

For most applications the HMMC-1002 can be driven by two complementary negative voltage ramps placed on V_1 and V_2. Some applications have additional requirements such as: single control voltage, improved VSWR, temperature compensation, and improved voltage versus attenuation linearity. The DC reference circuit on the HMMC-1002 attenuator chip can be used to satisfy these requirements.

As shown in Figure 1, the DC reference circuit is a non-distributed "T" attenuator designed to operate in a 500 Ω system and to track the control voltage versus attenuation characteristics of the RF attenuator. The driver that utilizes the DC reference circuit is shown in Figure 2.

Op amp 1 insures that the attenuator maintains a good input and output match to 50 Ω, while op amp 2 improves the linearity over that attainable when using only voltage ramps.

If optimum VSWR is all that is required, op amp 2 is eliminated while leaving R_L connected to DC_{OUT} on the HMMC-1002, and a negative control voltage is applied directly to V_2. As shown, a voltage reference is fed to both terminals of op amp 1 through 500 Ω resistors. (The voltage reference, V_{REF}, shown in Figure 2, is a positive voltage and will be discussed later.) For a positive reference the inverting terminal of op amp 1 is grounded through R_{REF} (which is ideally 500 Ω), while the noninverting terminal is grounded through the DC reference circuit by connecting it to the DC_{IN} port on the TC721. The reference circuit termination, R_L, is connected to the DC_{OUT} port and is also ideally 500 Ω.

At equilibrium, the voltages at nodes A and B must be equal which implies that the input impedance to the DC reference circuit is equal to R_{REF} . When V_2 is changed to a more negative voltage, the voltage at node A becomes greater than that of node B. This voltage difference causes the output voltage of op amp 1 to move toward its positive rail until equilibrium is once again established. When V_2 is changed to a less negative

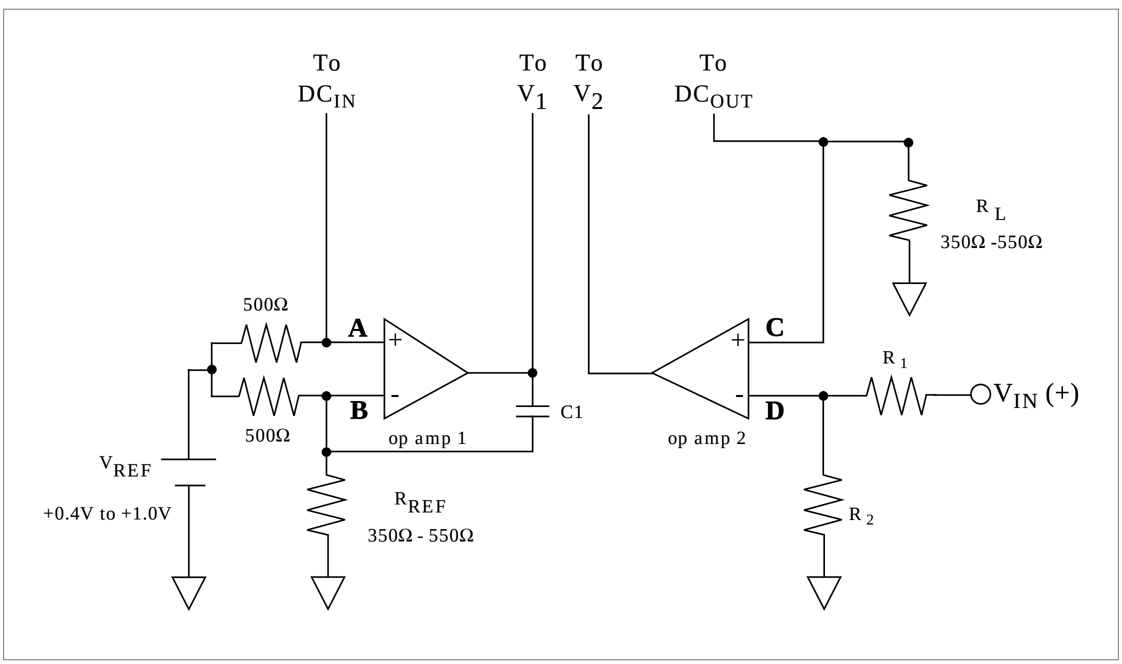

Figure 2. HMMC-1002 Attenuator Driver

value the voltage at node A becomes less than that of node B and the output voltage of op amp 1 will swing toward its negative rail until equilibrium is established. If the reference circuit precisely tracks the RF circuit, the voltage output of op amp 1 at equilibrium insures that the RF circuit is matched to 50 Ω when the reference circuit is matched to 500 Ω.

If attenuation linearity is required, op amp 2 is included as shown in Figure 2 and a positive control voltage is applied to V_{IN}. At equilibrium, nodes C and D are equal. When V_{IN} is changed, the output of op amp 2 adjusts to a value that forces the voltage at node C to equal the voltage at node D. Therefore, the output of the DC reference circuit is proportional to V_{IN}. This also makes $\log(V_{IN})$ proportional to $\log(DC_{OUT}/DC_{IN})$ where

$$20 \times \log(DC_{OUT}/DC_{IN})$$

is the attenuation of the DC reference circuit. If the FET parameters of the DC reference circuit track the FET parameters of the RF circuit, the voltage output of the RF circuit is also proportional to the control voltage. This translates into a linear relationship of the attenuation (in dB) versus $\log(V_{IN})$. Figure 3 shows two attenuation versus voltage curves for a HMMC-1002 device. These curves were obtained by using the driver circuit shown in Figure 2. One curve was obtained by using 0.7V for V_{REF} and the other curve was obtained by using 1.0V for V_{REF} .

Temperature compensation is provided by op amp 2 in Figure 2. Op amp 2 adjusts V_2 in such a way as to keep point C equal to point D. As the attenuation changes over temperature, point C tries to change, but is corrected by op amp 2.

B. Adjustments

Because the FETs in the DC circuit are not identical to those in the RF circuit, the DC circuit does not exactly track the RF circuit. This results in attenuation versus voltage curves that are not exactly linear. One way to minimize this effect is to use a positive reference. The optimum value for the positive reference voltage varies from wafer to wafer (due to process variations) but is usually between +0.4 Volts and +1.0 Volts.

Another way to improve performance of the attenuator driver circuit is to adjust R_L and R_{REF} . If the reference circuit precisely tracked the RF circuit and the ON resistance of the FETs was zero ohms, then R_L and R_{REF} would be 500 Ω.

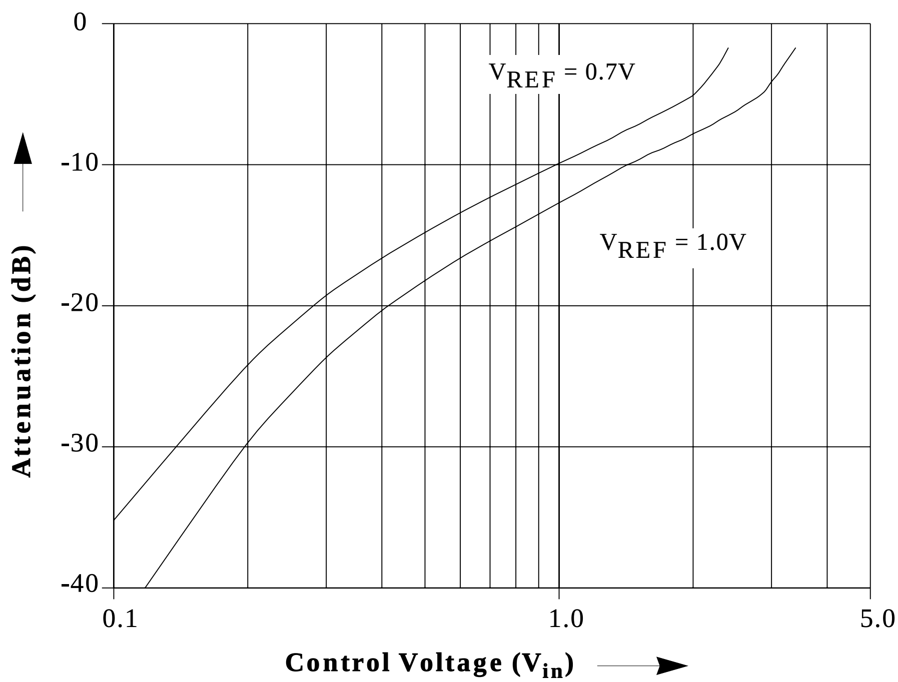

Figure 3. HMMC-1002 Attenuation vs. Control Voltage (V_{in}) @ 13.0 GHz

Due to the difference in layout structures, the reference circuit does not track the RF circuit precisely. R_L and R_{REF} are adjusted in order to compensate for these differences. Optimum values for R_L and R_{REF} have been found to be between 350 and 550 Ω. For maximum dynamic range on the attenuation control circuit, R_L should be less than R_{REF} by an amount equal to the ON resistance of the reference circuit series FETs. The ON resistance of the series FETs is about 70 Ω total. Therefore, the relationship between R_L and R_{REF} is as follows:

$$R_{REF} = R_L + 70\Omega$$

The voltage divider formed by R_1 and R_2 is used to adjust the sensitivity of the attenuator versus control voltage. For the driver circuit shown in Figure 2, maximum attenuation is always achieved by setting V_{IN} equal to 0 Volts. Minimum attenuation is achieved when

$$V_{\mathrm{IN}} \approx \left(\frac{R_1 + R_2}{R_2}\right) \times \left(\frac{R_{\mathrm{L}}}{500\Omega + R_{\mathrm{L}}}\right) \times V_{\mathrm{REF}}$$

or

$$V_{IN} \approx \left(1 + \frac{R_1}{R_2}\right) \times DC_{OUT}$$

Therefore, an increase in the resistor ratio R_1/R_2 increases the value of the control voltage required to produce minimum attenuation.

As mentioned previously, the suggested range for the reference voltage is +0.4 Volts to +1.0 Volts. If a negative reference voltage is used in place of a positive reference the polarities of the op amps must be switched, and the control voltage V_{IN} must be negative. The maximum suggested magnitude for a negative reference voltage is 0.6 Volts. The advantage of using a negative reference voltage is that a negative control voltage can be used to drive the linearizing control circuit without using an external inverter; the disadvantage is that the linearity of the attenuator and driver are slightly degraded.

C. Components

The OP-270, manufactured by Precision Monolithics, was used in the control circuit that produced the results shown in Figure 3; however, any low noise, low offset voltage op amp should produce similar results. Suggested supply voltages for the OP-270 are 3.6 Volts on the positive supply and -6 Volts on the negative supply. These low supply voltages keep the positive and negative rails of the OP-270 relatively close to the absolute maximum voltage levels of the control lines on the HMMC-1002 while providing enough power to the OP-270 for it to perform satisfactorily as an operational amplifier. If larger supply voltages are unavoidable, voltage clamps are needed between the output of the operational amplifiers and the V_1 and V_2 control line inputs to prohibit large control voltages from damaging the HMMC-1002.

D. Circuit Limitations

The driver circuit has some limitations and a few potential trouble spots. One of the potential trouble spots is a tendency to oscillate if not properly compensated. The capacitor C1 (shown in figure 2) was used as a lead compensation network. A value of 220pF was used for the OP-270. If other op amps are used, this value may need to be adjusted.

One of the limitations of the circuit is switching speed. The op amps were the limiting factor in the breadboard circuit that was built at MWTC. Faster op amps are available, but care must be taken in order to prevent the circuit from oscillating.

IV. Appendix – Quick Review of Matched T-Attenuators

A. Simplified Schematic for TC721

Figure 4 is a simplified schematic of a DC-equivalent T-Attenuator circuit for the HMMC-1002 where the FETs are represented by variable resistors.

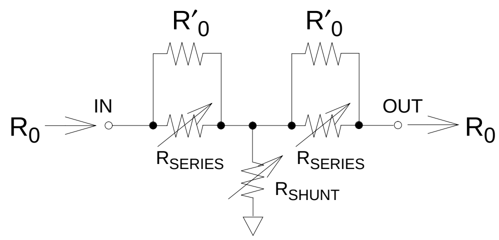

Figure 4. HMMC-1002 Simplified Schematic

B. Resistor Values as Functions of Attenuation

With the constraints that the output is loaded by R_0 and the input resistance will be R_0, one can derive the value of the parallel series resistors as

$$R'_0 \parallel R_{\mathrm{SERIES}} = \frac{(A-1)}{(A+1)} R_0$$

or (for $R'_0 = R_0$)

$$R_{\mathrm{SERIES}} = \frac{(A-1)}{2} R_0$$

and the value of the shunt resistor as

$$R_{\mathrm{SHUNT}} = \frac{2A}{(A^2-1)} R_0$$

where

$$A \equiv \frac{V_{\mathrm{IN}}}{V_{\mathrm{OUT}}}$$

i.e., A is the voltage ratio and the attenuation in dB is $20 \log_{10}(A)$.

Figure 5 is a plot of the resistor values versus attenuation.

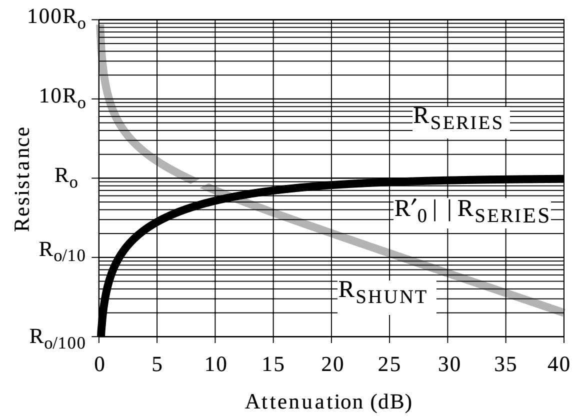

Figure 5. T-Attenuator Resistor Values

C. Maximum Power Dissipation

It can be shown that:

1. Resistors R_{SERIES} have maximum dissipation when $A = 3$ (or 9.54 dB) where $R_{\mathrm{SERIES}} = R_0$.
2. Resistor R_{SHUNT} has maximum power dissipation when $A = 1 + \sqrt{2}$ (or 7.66 dB) where $R_{\mathrm{SHUNT}} = R_0$.
3. Resistors R'_0 have maximum power dissipation at maximum attenuation (in the limit as $A \rightarrow \infty$).

For additional information contact Gordon DeWitte at (707) 577-3887 or Wes Whiteley at (707) 577-5292.

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