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2-26.5 GHz Variable Gain Amplifier Using HMMC-5021/22/26 and HMMC-1002 GaAs MMIC Components

Application Note # 31

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Abstract

A review of a broadband 2 to 26.5 GHz variable gain amplifier is presented. This amplifier was constructed to demonstrate the performance characteristics of two MWTC MMIC components: the HMMC-5021/22/26 TWA, and the HMMC-1002 broadband attenuator. Measured results on small-signal characteristics, large-signal power and gain, and harmonic distortion are presented in order to communicate the potential performance characteristics and limitations of these devices.

1.0 Introduction

The following paper describes a broadband, multistage GaAs MMIC amplifier characterized over the full 2-26.5 GHz frequency range. This amplifier features 30 dB of tunable gain control and is capable of delivering 20 dBm output power to 20 GHz, and a minimum gain of 20 dB to 26.5 GHz. Maximum flatness obtainable is ±1 dBm from 2-26.5 GHz. The harmonics under near-saturation conditions are -25 and -30 dBc for second and third harmonic levels, respectively, at fundamental frequencies to 8 GHz.

2.0 Assembly and Topology

The design of this three stage amplifier is based on two GaAs MMIC components currently being produced by MWTC. The first is the HMMC-5021/22/26 traveling wave amplifier which provides approximately 8 dB gain to 26.5 GHz and is available in chip form. Three HMMC-5021/22/26s are cascaded in series to provide the amplifier gain. The amplifier block diagram is shown in Figure 1. Tunable gain is achieved via a HMMC-1002 broadband (50 GHz) attenuator that proceeds the HMMC-5021/22/26s. The HMMC-1002 has 30 dB of dynamic range at 1 GHz, and increases to approximately 35 dB at 26.5 GHz and 40 dB at 50 GHz.

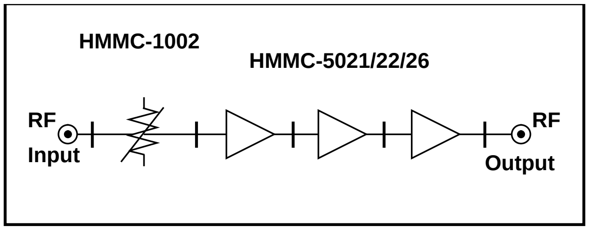


Figure 1.
Broadband amplifier block diagram

The amplifier topology, illustrated in Figure 2, consists of an input thin film circuit with a 50Ω transmission line, followed by the HMMC-1002, and then the cascaded series of HMMC-5021/22/26 TWAs, each separated by 50Ω transition circuits. The thin film circuits are all fabricated on 10 mil sapphire substrates and include 10 pf beam lead DC block capacitors.

The lengths of the input and transition circuits are kept short to control the in-band ripple. The output circuit is a longer 50Ω thru-line, which is used to fill in the extra space in the package. In other amplifier configurations this extra space can accommodate additional stages, and other circuits such as gain slope compensation circuits and filters. All active components are soldered to moly shims which are then epoxied onto the carrier.

The package includes ten DC feedthrough capacitors, five on a side. Two are used to the V_1, V_2 controls on the HMMC-1002, and six are used for the gate and drain biases for the HMMC-5021/22/26s. Over voltage protection is included in the drain bias circuitry, with the addition of ten volt zener diodes, and 68 pf shunt chip capacitors. A bipolar controlled bias board is employed to pass DC bias to the packaged amplifier, and allows independent monitoring of all voltages and currents to each stage. This bias board is specifically designed to mate to the test package and the entire package/bias board assembly is mounted on a large heat sink for proper heat dissipation.

3.0 RF Performance

A. Small Signal Performance

Although this amplifier was originally intended to deliver satisfactory RF performance to 20 GHz, the amplifier provided excellent performance to 26.5 GHz. Initially dubbed the "*20-20-20 Amp*," the amplifier goals included a minimum of *20* dB gain and *20* dBm output power to *20* GHz. However, at first turn-on the amplifier delivered a minimum gain of over 23 dB from ~800 MHz to 26.5 GHz. Figure 3 shows the small-signal gain ($|S_{21}|$) vs. frequency for various attenuator settings. The TWAs are biased to 150 mA/stage with seven volts on the drain. Since the I_{DSS} of the TWAs was ~160 - 170 mA, only a slight negative voltage on the gate line was required to achieve the desired operating current.

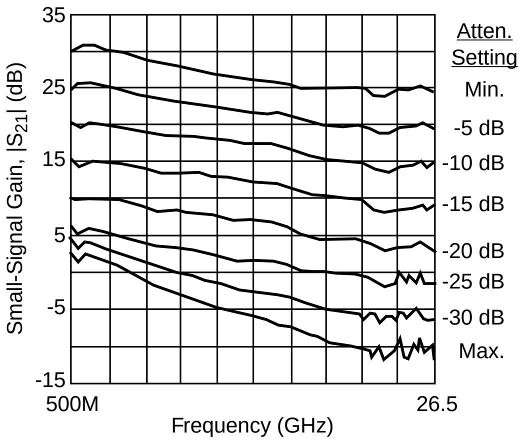


Figure 3.
Amplifier small-signal gain vs. frequency for various attenuator settings.

The attenuator was first adjusted to minimum attenuation to record the maximum gain of the amp and determine the gain slope. Then, the attenuation was incremented in 5 dB steps while maintaining this same gain slope to measure the

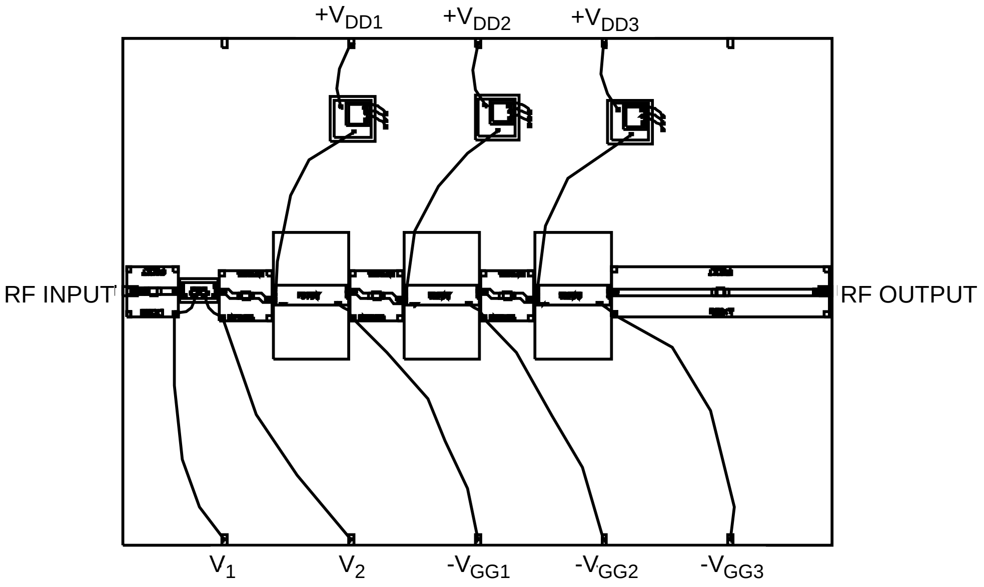


Figure 2.
Amplifier Topology.

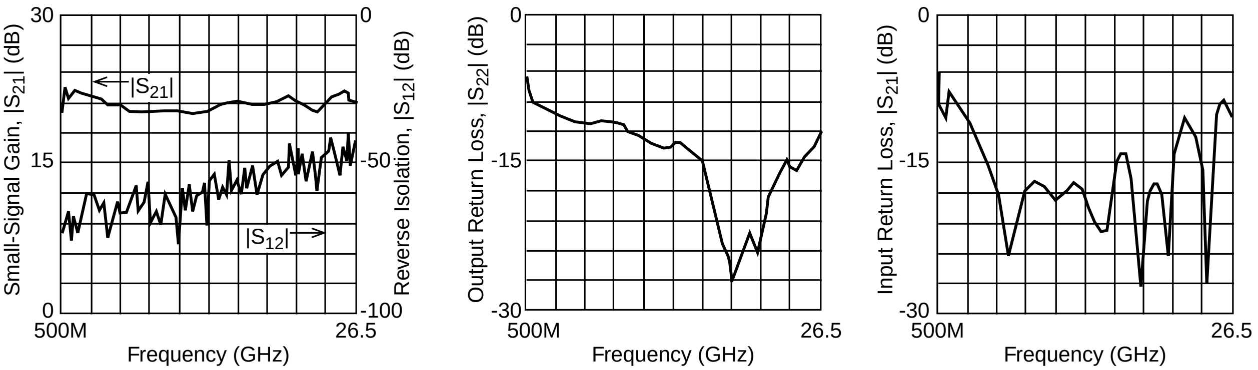
broadband dynamic range. At minimum attenuation, the maximum gain was 30.9 dB @ 1.9 GHz, and the minimum gain was 23.7 dB @ 23.1 GHz. This yields a gain slope of ~7 dB (or a gain flatness of ± 3.5 dB) across the band. Additional gain measurements were recorded as the attenuation was increased while maintaining the same gain slope. At maximum attenuation the gain slope increased to about 14 dB (± 7 dB) with a maximum gain of 2.2 dB @ 1.6 GHz. The dynamic range at 1.6 GHz is ~29 dB, and the maximum dynamic range occurred around 23 GHz, with a value over 35 dB.

No attempt was made to extend the low frequency performance of the amplifier below 800 MHz. The low frequency performance is limited mainly by the small 10 pF interstage blocking capacitors. The high frequency performance actually extends beyond 26.5 GHz but, due to test set limitations, was not measured.

The gain slope measured agrees with the initial expectations and can be calculated based on the size of the package, the flatness characteristics of the HMMC-5021/22/26s, and the insertion flatness of the HMMC-1002 at minimum attenuation. The package length is approximately 28.5 mm from inner wall to inner wall, and with 50Ω thru lines and transition circuits, the package gain slope, including the SPC 3.5 mm connections, is ~ 2 dB. Since both DC and small-signal data was available on each TWA, three devices were selected with a 2-26.5 GHz gain slope of 1 dB. At minimum attention setting, the attenuator has a slope around 2 dB across the band. Therefore,

$$\begin{aligned} \text{Total Gain Slope} &= Slope_{pkg.} + 3\,(Slope_{HMMC\text{-}5021/22/26}) + Slope_{HMMC\text{-}1002} \\ &= 2 + 3(1) + 2 \\ &= 7\ dB. \end{aligned}$$

The attenuator can be used to compensate for the intrinsic gain slope of the amplifier via the independent control voltages, V_1 and V_2. However, this will result in poorer input and output return loss of the HMMC-1002 at some frequencies. Figure 4(a) through (c) shows the small-signal response of the amplifier with $S_{21} > 20$ dB, and with the attenuator adjusted to yield the flattest gain from 2 to 26.5 GHz. In Figure 4(a) the gain is greater than 20 dB across the entire band, and the worst case gain flatness is ±1 dB. The attenuator has been adjusted to yield a pseudo *positive* gain slope to compensate for the 7 dB slope described previously. In reality, this is achieved by creating a greater low-frequency mismatch at the input of the attenuator, as seen in Figure 4(b). Under these conditions, the worst case input match between 2 and 26.5 GHz was -9.3 dB, and occurred at 2 GHz. The worst case output match was -8.4 dB which also occurred at 2 GHz. Since the input match is dominated by the attenuator, a direct performance trade-off



4 (a) 4 (c) 4 (b)

Figure 4.
Small-signal amplifier response with attenuator adjusted to yield max. flatness; (a) Gain and reverse isolation, (b) Input return loss, and (c) Output return loss.

can be seen between the overall amplifier flatness and the broadband input response of the attenuator.

The output return loss of the amp under these same conditions is shown in Figure 4(c). Here the response is dominated by the last HMMC-5021/22/26 stage, the output connector center pin-to-substrate transition, and the output thin film circuit. The poorer return loss at lower frequencies is due to two major factors: the DC blocking capacitance value (10 pf), and the inductance associated with drain bias bond to the HMMC-5021/22/26. The recommended length of the drain bias bond is approximately 250 mils. If the bond is too short, the TWA drain line does not see enough inductance at the drain termination to look like an open circuit at low frequencies. If the bond is too long, the bond may droop mid-span and potentially lead to a mechanical stress problem where the bond could short to the package floor. The best return loss will be achieved for bond lengths which model as open circuits at the drain bias pad at the frequency of interest. The multiple ripples in the output response are caused by a number of factors: the number of stages, the length of the thin film circuits, the re-reflection of the RF signal “bouncing” off the input and output of the TWAs due to mismatch, and the inductance of the drain bias bond wire. In this amplifier, the output circuit is over 8 mm long, and the mismatch between the output RF connector pin and this circuit degrades the output match slightly.

In-band gain ripple is another by-product of mismatch loss. Shorter thin film transition circuits and smaller overall package length help to reduce the ripple. Radiative coupling between drain bond wires and adjacent TWAs is another mechanism which contributes to gain ripple. Most of the remaining gain flatness variation seen in Figure 4(a) is due to the combination of these two factors. To reduce the effects of radiative coupling, polyiron was placed between each drain bond and as close to each HMMC-5021/22/26 stage as possible. This reduced the ripple from 1.5 dB to 1 dB. Optimum reduction in ripple can be achieved by designing a polyiron section pre-shaped to lie beneath and around each drain bond, and by adding an additional sheet inside the package cover.

B. Large-Signal Performance

The amplifier was tested at large input drive levels to determine the saturation characteristics. Figure 5 shows the gain vs. output power characteristics for various attenuator settings at 18 GHz with the HMMC-5021/22/26s biased to seven volts @ 150 mA/stage. The saturated output power is dominated mainly by the last TWA stage in the amplifier. Output powers at -1 dB gain compression were greater than 18 dBm, independent of the attenuator setting. Under saturated conditions, the middle two HMMC-5021/22/26 stages are still operating small-signal. The maximum forward gate-current drawn by the last HMMC-5021/22/26 stage was under 1 mA at 5 dB compressed gain. At this drive level, I_{DS}(Q3) decreased from a quiescent level of 150 mA to 107 mA. Power reversal was observed at the minimum attenuation setting when the amplifier was driven beyond 3 dB gain compression.

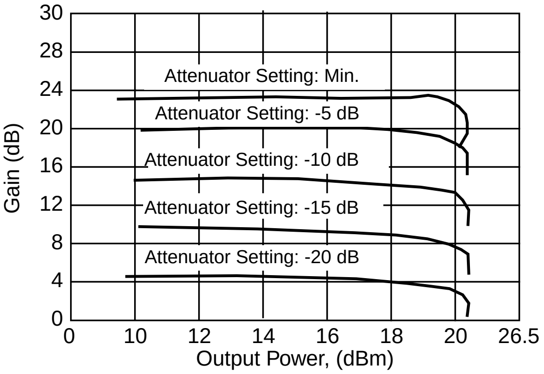


Figure 5.
Gain vs. output power at various attenuator settings. Measured at 18 GHz, V_{DS} = 7V, I_{DS}(Q) = 150 mA/stage.

C. Harmonic Performance

The 2nd and 3rd harmonics of the amplifier were measured under standard bias conditions and with a leveled output power slightly below saturation. The output power at the fundamental was fixed at 17 dBm, which is ~3 dB below the -1 dB compression point. The measured harmonics, shown in Figure 6, were recorded with an HP8566 spectrum analyzer. Since the 8566 can measure to 21 GHz, the fundamental frequency was stepped from 2 to 8 GHz, yielding a second and third harmonic sweep from 4 to 16 GHz, and 6 to 24 GHz, respectively. The second harmonic increases from -35 to -25 dBc across the fundamental band. The 3rd harmonic increases from -42 to -30 dBc. The attenuator control voltages were adjusted to give a flat 20 dB amplifier gain across the band. Since TWAs from a wafer with typical values of pinch-off voltage and saturated drain current were used in this amplifier, the resulting harmonic performance is believed to be typical.

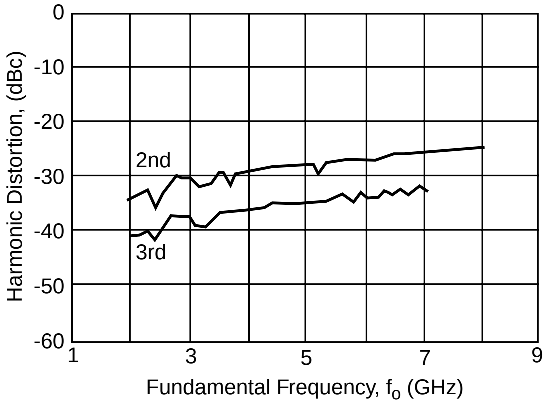


Figure 6.
Second and third harmonic performance for 2 $\leq f_0 \leq$ 8 GHz, Bias: 7V @ 150 mA/stage. $P_{out}(f_o)$ = 17 dBm.

4.0 Summary

A broadband four-stage variable gain amplifier has been constructed using HMMC-5021/22/26 and HMMC-1002 GaAs MMIC components. The amplifier delivers 20 dBm saturated output power to 20 GHz, and a minimum of 20 dB gain to 26.5 GHz. The worst case input and output return loss is less than -8.5 dB over the full 2-26.5 GHz bandwidth. The HMMC-1002 attenuator provides the amplifier with a broadband dynamic range in the 30 to 35 dB range. Second and third harmonics are approximately -25 and -30 dBc across a fundamental frequency range of 2 to 8 GHz. In its current configuration, the attenuator can be adjusted to yield an overall amplifier flatness and reduced in-hand ripple can be achieved by the addition of gain slope compensation circuits and polyiron.

The amplifier is intended to demonstrate a few of the performance characteristics of the HMMC-5021/22/26 and HMMC-1002 devices. The results reported in this application note were obtained from one amplifier. An amplifier being designed for use in test instrumentation would require much more characterization to determine the appropriate amplifier specifications. The small-signal results obtained are consistent with the current distributions and specifications on the HMMC-5021/22/26. A designer would be well advised, however, to replace the output stage with a TC702 Power TWA to consistently attain this level of large-signal performance.