An SPDT PIN Diode T/R Switch for PCN Applications

Application Note 1067

Introduction

The PCN (**P**ersonal **C**ommunications **N**etwork) market has shown dramatic growth in the past several years, and promises to expand even more rapidly before the end of the decade. Hand held terminals providing voice and data transmission in cells smaller than those used for cellular telephone are either in the design phase or undergoing trials in Europe, Japan and the U.S. Various frequency bands are being used, but most of the activity is taking place in the range of 1.7 to 2.0 GHz. This paper describes a 1750 MHz SPDT T/R (**T**ransmit/**R**eceive) antenna switch suitable for such a hand-held terminal. The design concepts contained in this paper can be applied to other frequency bands as well.

Design Requirements

An SPDT T/R antenna switch carries with it a unique set of design requirements when it is being designed for a battery operated application. In addition to the usual specifications for good match and low loss, the following requirements apply:

- Very low or zero current consumption while in the standby or receive mode.
- Moderate current consumption while in the transmit mode.
- High isolation in the receiver arm to protect the front end from damage when the transmitter is operating.
- Sufficient isolation in the transmit arm to isolate the receiver from variations in the transmitter's output impedance.
- Small size.
- Low cost.
- Surface mountable.

From a reading of these requirements, it is clear that this type of SPDT switch is not necessarily symmetrical. For example, 10 dB of isolation in the transmit arm is sufficient to prevent any variation in the output impedance of the transmitter (when in standby mode) from affecting the performance of the receiver. However, to protect the receiver ($P_{in} < +10$ dBm) from being damaged by a 1 Ω transmitter, more than 20 dB of isolation will be required in the receiver arm. Putting numbers to these design requirements results in the specification shown in Table 1.

This set of specifications, then, formed the design goal for the SPDT T/R switch described below.

Design Approach

In order to conserve bias current in the standby or receive mode, a switch of the type shown in Figure 1 can be used. When zero (or a small positive) voltage is applied to the bias port, both PIN diodes are in the high resistance (reverse biased) state. This isolates the transmitter (Tx) from the antenna,

Table 1. Specifications for SPDT T/R Switch

Requirement	Transmit Arm	Receive Arm
Insertion Loss, dB	<1	<1
Isolation, dB	>10	>25
Return Loss, dB	>15	>15
Bias current, mA	minimum	zero

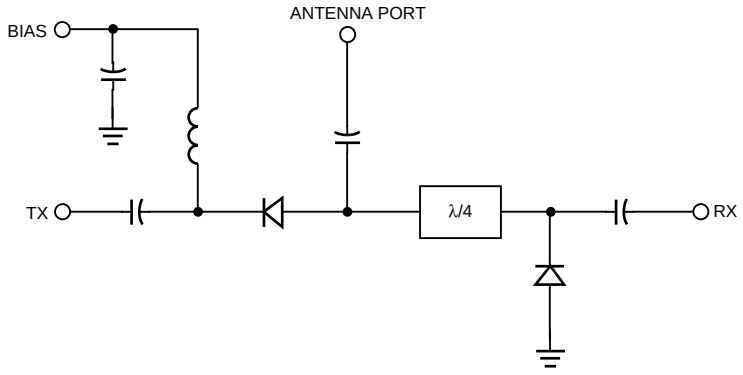


Figure 1. Low Current T/R Switch.

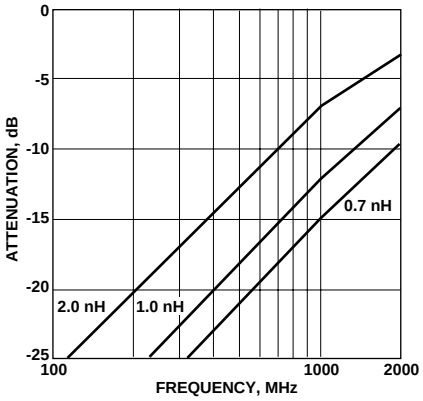


Figure 2. Attenuation vs. Frequency, Inductor Shunting a 50 Ω line.

and connects the receiver (Rx) to it. The application of a negative voltage to the bias port causes current to flow through both diodes. This puts the diodes into their low resistance (forward bias) state, connecting the transmitter to the antenna and isolating the receiver. Such a design approach, using a λ/4 section to transform the short circuit formed by the shunt diode to an open circuit at the common junction, will operate only over a limited bandwidth. However, good performance will be obtained over a 20% to 30% bandwidth, more than sufficient for most applications.

Note that having the diodes in series in the bias circuit conserves current, compared to operating them in parallel.

Diode Limitations

PIN diode switches, operating in the frequency ranges of HF through millimeter waves, have been produced for years. However, in an application such as this one, cost considerations require that plastic packaged surface mount diodes be used in some type of planar transmission line. The SOT-23 package has become a virtual industry standard, and is the type which is described in this note. Unfortunately, the SOT-23 package leads and bondwire add approximately 2.0 nH of parasitic inductance to the diode. As can be seen in Figure 2, even an ideal diode (R = 0 Ω) with this much inductance will produce less than 5 dB of isolation when mounted in shunt in a 50 Ω system.

The HSMP-4890 PIN diode overcomes the problem of excessive parasitic inductance in the SOT-23 by using two leads for the anode contact, as shown in Figure 3. This diode is a special low inductance variation of the standard HSMP-3890 series. Measured inductance for this product is ≅ 1.0 nH, half the usual value. Reference to Figure 2 will show that this results in an improvement in isolation compared to a conventional diode. However, isolation in the PCN band is still less than 10 dB, and other methods must be sought to bring the receiver arm isolation up to the required value.

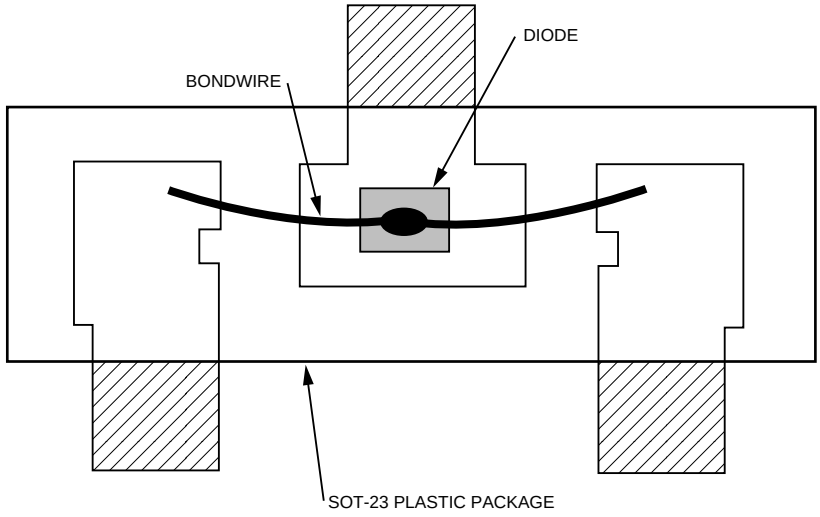


Figure 3. HSMP-4890 Low Inductance Diode.

Circuit Design Approach

Two circuit design "tricks" can be used to extract sufficient isolation from the shunt HSMP-4890 diode. The first is to substitute CPW (**C**o**P**lanar **W**aveguide) transmission line for the familiar microstrip. Described in Appendix A, this planar transmission medium offers the advantage of having ground on the same (top) surface of the board as the conductor. When the HSMP-4890 is mounted such that it straddles the CPW, as shown in Figure 4, the availability of ground potential within 0.006" of both sides of the center conductor reduces the parasitic inductance of the HSMP-4890 to ≅ 0.7 nH. From Figure 2 it can be seen that an ideal shunt diode with this value of inductance produces more than 10 dB of isolation in the PCN band. Thus, CPW was chosen over microstrip for the design of this switch.

In order to insure that a SOT-23 package can straddle a CPW, the sum of the linewidth plus both gap widths must be less than 0.055 inch. A design curve[1] for such a CPW on **HT-2** PCB material is given in Figure 5. See Appendix B for a discussion of **HT-2** PCB material, which was chosen over the more familiar FR-4 in order to minimize losses.

The second circuit approach which can be used to realize sufficient isolation in the receiver arm is to use two shunt diodes separated by 90° of electrical length. If a single shunt diode will produce 11 dB of isolation at 1.75 GHz, then two in cascade with 90° between them will exhibit (2 x 11) + 6 = 28 dB. At frequencies which are lower than those discussed here, a lumped element phase delay circuit such as

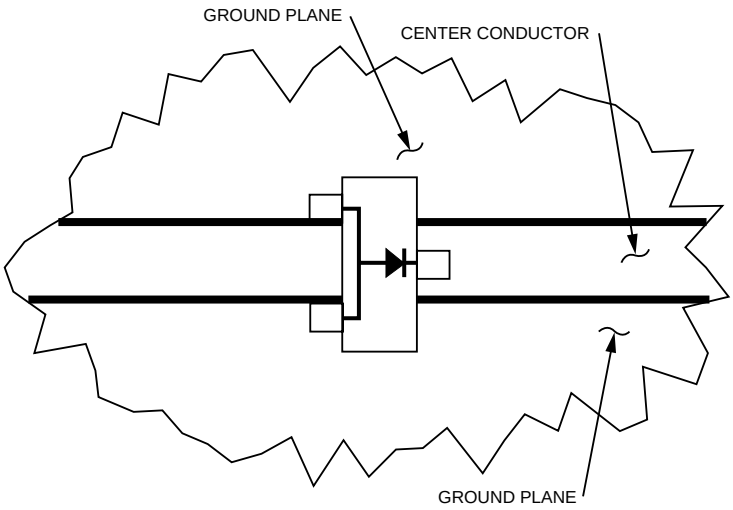


Figure 4. HSMP-4890 Diode Mounted in Shunt Across a CPW.

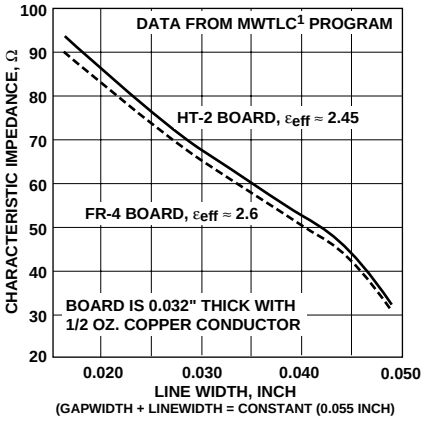


Figure 5. Impedance vs. Linewidth, CoPlanar Waveguide.

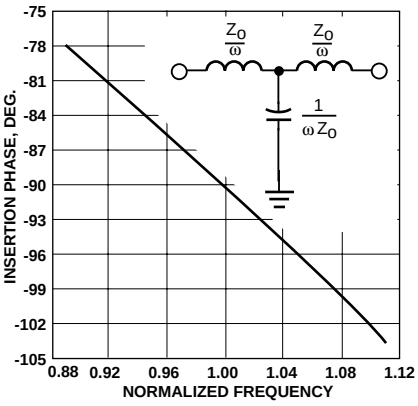


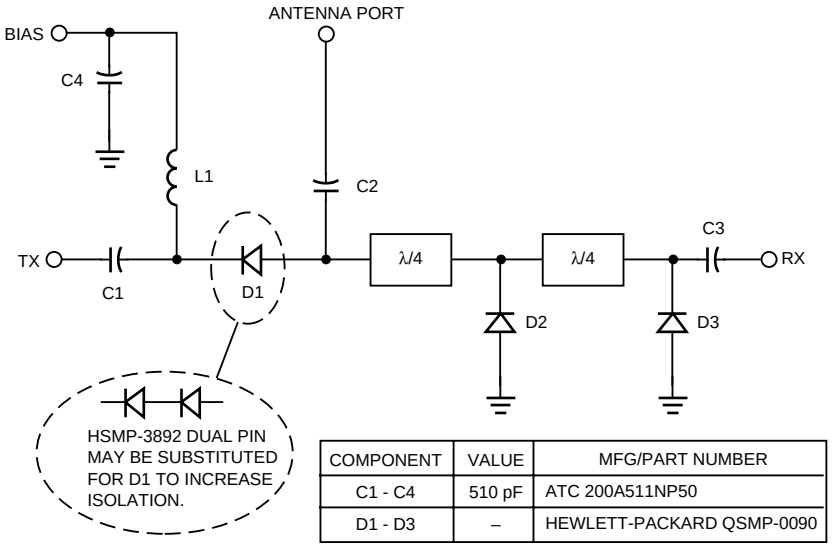
Figure 6. 90° Phase Delay Circuit.

that shown in Figure 6 would offer low losses and compact size. However, as frequencies approach 2 GHz, the losses in inductors (and, to a lesser extent, capacitors) become excessive and λ/4 transmission lines become more attractive.

Using this combination of diode and circuit design elements, the switch shown schematically in Figure 7 was designed, laid out and fabricated.

Circuit Layout and Component Selection

At frequencies above 1 GHz, care must be taken to avoid unnecessary losses in any circuit. Before the final layout of the switch was undertaken, therefore, the initial design was modelled and analyzed using MMICAD®[2]. In particular, it was found that the distance from series diode D1 to the switch common junction had a significant effect upon the reverse bias insertion loss in the receive arm. This distance was, therefore, kept to an absolute minimum. An air



COMPONENT	VALUE	MFG/PART NUMBER
C1 - C4	510 pF	ATC 200A511NP50
D1 - D3	–	HEWLETT-PACKARD QSMP-0090

Figure 7. Schematic of the prototype Switch.

core solenoid was selected for L1, in that it provided 50 nH of inductance with high Q and low cost. Since this is a surface mount design, chip capacitors were selected for bypassing and bias blocking. However, it was found that many chip capacitors which show good performance at VHF frequencies can exhibit losses of 0.2 to 0.3 dB each when they are used for bypass and blocking devices in the PCN band. Several different types were characterized before those shown in Figure 7 were chosen. In order to save board space, the λ/4 50 Ω line between D2 and D3 was folded upon itself.

The physical layout of the switch is shown in Figure 8. Finished width and length were 1.6" x 1.8".

CPW brings with it a number of layout requirements which are unique. It is essential that the grounds on both sides of the conductor are maintained at the same potential. The two anode leads of D2 and D3 serve the purpose of providing a bridge between ground planes in the switch's only long transmission line. The common junction deserved some special attention because it is a TEE junction. Three via holes were used to connect the three ground surfaces to a triangular interconnecting patch on the otherwise blank underside of the board, as can be seen in Figure 8. Alternatively, the ground plane could have been interconnected on the top surface and the conductors interconnected on the underside, as shown in the lower inset. This need to maintain symmetry in a CPW circuit is illustrated by the use of a pair of capacitors to realize the bypass C4. If only one is used, touching the bias conductor at the input will induce ripples in the passband response of the switch.

Finally, any circuit realized in CPW must, at some point, interface with conventional microstrip. A straightforward transition between the two lines is shown in Figure 9, where twin via holes are used to connect the two overlapping groundplanes.

Measured Performance

The switch shown in Figure 8 was fabricated and fitted with E.F. Johnson 142-0701-801 SMA connectors. These end launchers have ground fingers in the same plane as the connector's center conductor, making them ideal for use with CPW.

Before final measurements were made, a HSMP-3892 PIN diode pair (two diodes, connected in series in a single SOT-23 package) was substituted for series diode D1 shown in Figure 8. This was done to increase the transmitter arm isolation by halving the effective reverse bias capacitance of D1. The layout of the circuit board allows physical interchangeability between the HSMP-3892 and the HSMP-4890 products.

Data obtained from the prototype switch are given in the swept frequency measurements of Figures 10 through 13. As can be seen from all four data plots, return loss at 1750 MHz is greater than 15 dB at all ports for both bias conditions (+5 V and -20 mA). Receiver arm isolation is 28 dB at the design frequency, and the transmit arm isolation is 15 dB. Insertion loss for the same two arms is 0.8 dB and 0.7 dB respectively.

The measured value of transmitter arm isolation was well above the 10 dB originally specified. Use of the HSMP-4890 (or standard product HSMP-3890) for the HSMP-3892 dual diode in the D1 series diode position would result in a reduction in isolation to ≅ 12 dB, a value which would be satisfactory for many applications. This might be considered by those manufacturers for whom it is important to

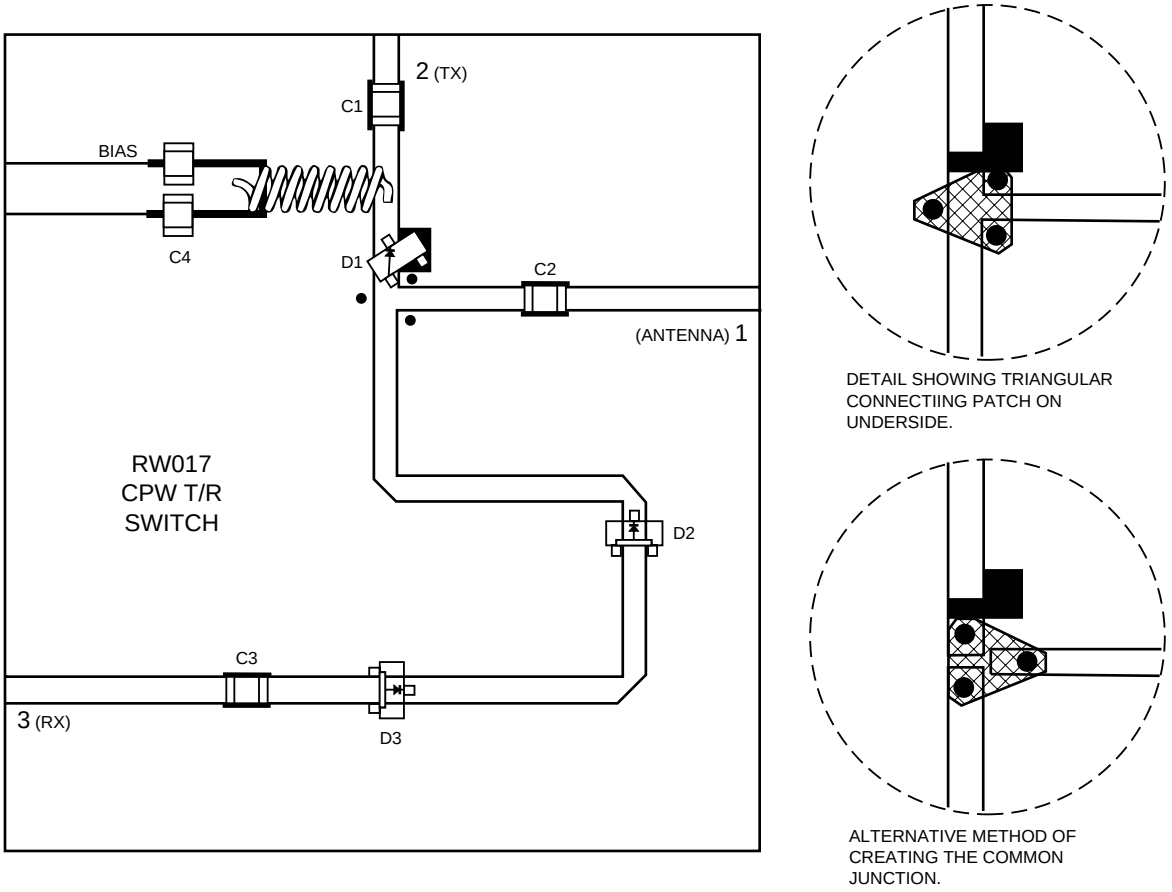


Figure 8. Layout of the T/R Switch.

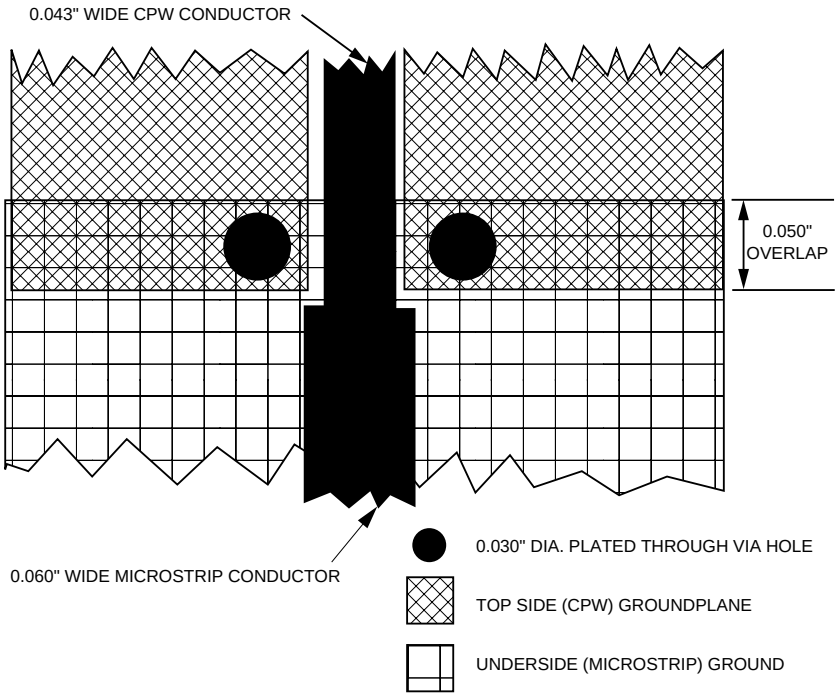


Figure 9. Microstrip to CPW Transition on 0.032" HT-2.

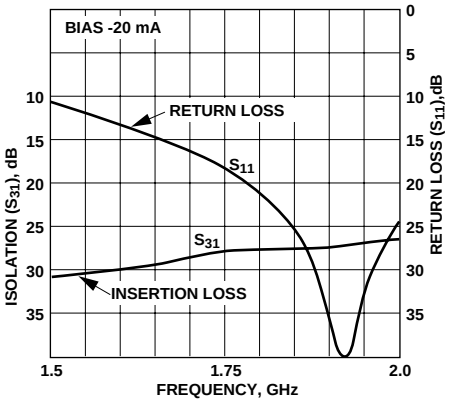


Figure 10. Receiver Arm Isolation.

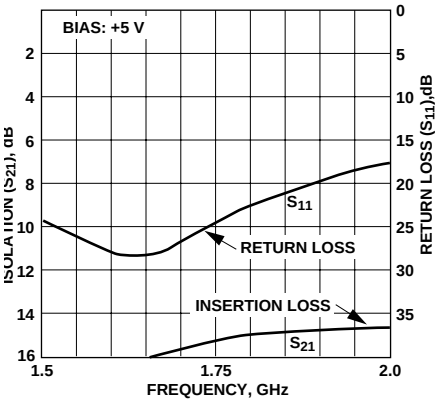


Figure 11. Transmitter Arm Isolation.

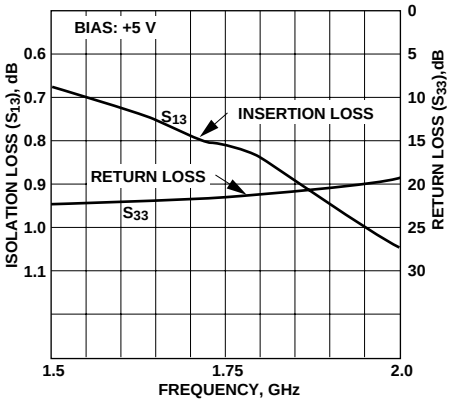


Figure 12. Receiver Arm Insertion Loss.

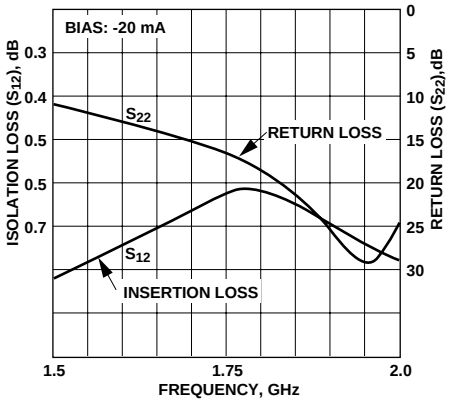


Figure 13. Transmitter Arm Insertion Loss.

minimize the number of different diode part numbers kept in stock.

Conclusion

An inexpensive, low power consumption SPDT switch for PCN hand-held applications has been described, along with design concepts based upon CoPlanar Waveguide and a new, low inductance PIN diode. The design approach contained in this paper is easily scaled to other frequency ranges.

Appendix A: CoPlanar Waveguide

What Is Coplanar Waveguide?

CoPlanar Waveguide (CPW)[3,4,5,6,7,8] is a RF-microwave transmission line having all conducting elements on the same side of a suspended substrate. A CPW transmission line consists of a center strip conductor with semi-infinite groundplanes running in parallel on both sides, separated from the center conductor by a width of exposed dielectric material. See Figure 14. Analytical expressions for the characteristic impedance (Z_o) and effective dielectric constant can be obtained if the two slots are modelled as magnetic walls. If we assume the metallization thickness to be zero, the overall line capacitance per unit length can be computed as the sum of two capacitances; the

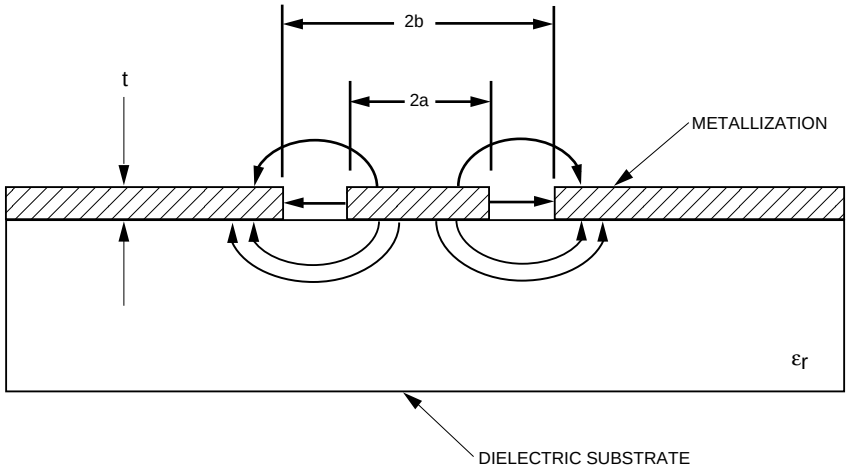


Figure 14. Cross-Section of CoPlanar Waveguide.

upper half with ε_o and the lower half with ε_r. The phase velocity (v_p) is

$$v_p = \frac{c}{\sqrt{\varepsilon_{eff}}}$$

where c = the speed of light in a vacuum

and

$$\varepsilon_{eff} \cong \frac{\varepsilon_r + 1}{2}$$

The characteristic impedance of a transmission line is

$$z_o = \frac{1}{Cv_p}$$

where C = line capacitance

Thus, within reasonable limits, the characteristic impedance is unaffected by substrate thickness, and is solely dependent upon the ratio a/b. The effective dielectric constant ε_{eff} is also relatively independent of Z_o, unlike the case with microstrip.

Why Use CPW?

CPW offers several advantages over the more commonly used microstrip layouts. The most significant of these are shunt connections that are easy to make as series connections, elimination of costly via holes or wraparounds, low radiation loss and insensitivity to substrate thickness. On the down side, CPW does have higher ohmic losses due to the concentration of its currents near the metal edges, though this does not pose much of a problem at lower microwave and RF frequencies. The surface mounting of devices on CPW imposes thermal constraints since it is a suspended substrate. This problem can be minimized by the improved thermal characteristics of some new materials (such as aluminum nitride) or the use of conductor backed CPW.

What Are Reasonable Limits?

As mentioned above, Z_o is relatively independent of substrate thickness, within reasonable limits. This assumption holds true provided that D > 2b (see Figure 15). In order to treat the ground planes as semi-infinite, and therefore be able to neglect them, S1 > 3b. Reducing the width of the ground planes leads to increases in Z_o. Another desirable simplification is that upper and lower metal covers have no effect upon Z_o. This will be the case if H1 > 4b and H2 > 3b. When these limits are exceeded, the effect of the upper and lower lids will be to lower Z_o. Line to line coupling is obviously dependent upon the width of the ground plane between them. A safe rule of thumb to follow is to maintain S2 > 5b to avoid unwanted coupling between parallel conductors.

Some Practical Tips On Designing With CPW

Since most circuits are likely to consist of more than a single transmission line, there are some basic guidelines to follow when laying out CPW circuits. Since the ground plane is on the same

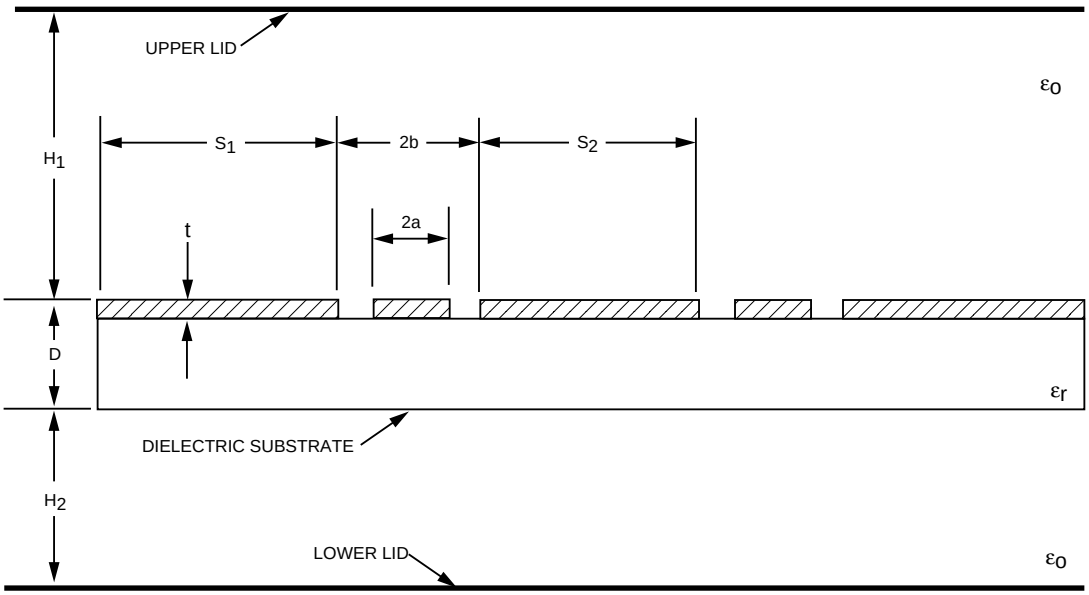


Figure 15. CoPlanar Waveguide with Top and Bottom Covers.

surface as the transmission lines it is very important to keep all of the ground planes at the same potential. This can be done through the use and proper spacing of conductive bridges (see Figure 16). Any time there is an intersection of conductors, or open or short circuit stubs, care must be taken to ensure that the ground planes remain at the same potential on both sides of the center conductor. This is accomplished through the use of conductive bridges, as shown in Figure 17. The same problem arises for bends in transmission lines. The best solution is to break the line at the bend, allowing metallization on the substrate to connect the ground planes, and use a conductive bridge to join the transmission lines. See Figure 18 for an illustration. Alternatively, one can use a ground plane conductive bridge in a manner similar to that illustrated in Figure 17 to force ground potentials to be equal at both ends of the bend.

It should be kept in mind that, for CPW formed on plastic laminate boards such as FR4, conductive bridges are most easily formed using plated through holes to connect to a small etched line on the underside of the board.

The effect of TEEs, intersections, and abrupt changes in linewidth (Z_o) is to add discontinuities to the CPW line which must be taken into account in the design of high frequency circuits. For example, in an open circuit shunt stub such as that shown in Figure 17, the short section of transmission line immediately on either side of the stub has a transverse field normal to G2 but not to G1. This can be modelled as a short section of high impedance line of $Z_o \cong 110\ \Omega$. If the open circuit stub is symmetrical with respect to the center

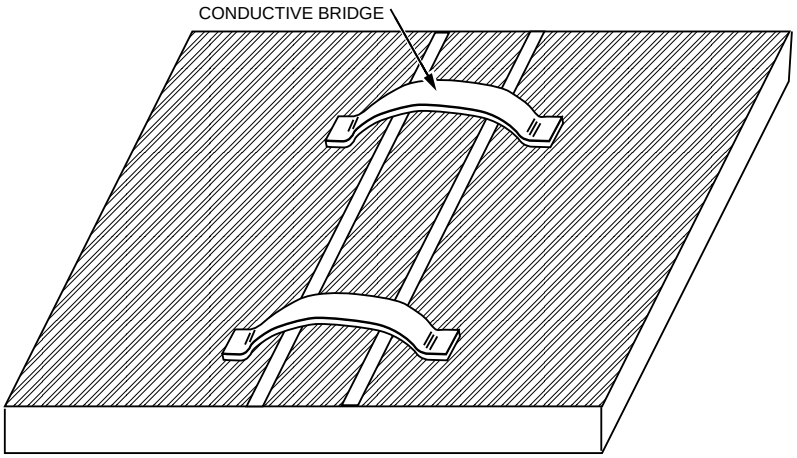


Figure 16. CPW with Conductive Bridge.

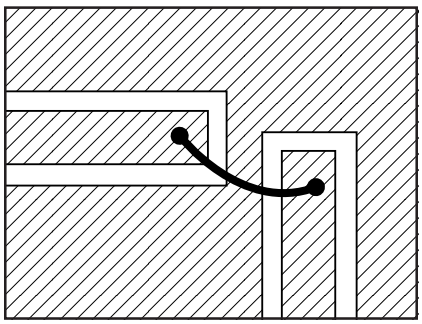


Figure 18. Ground Continuity is Maintained.

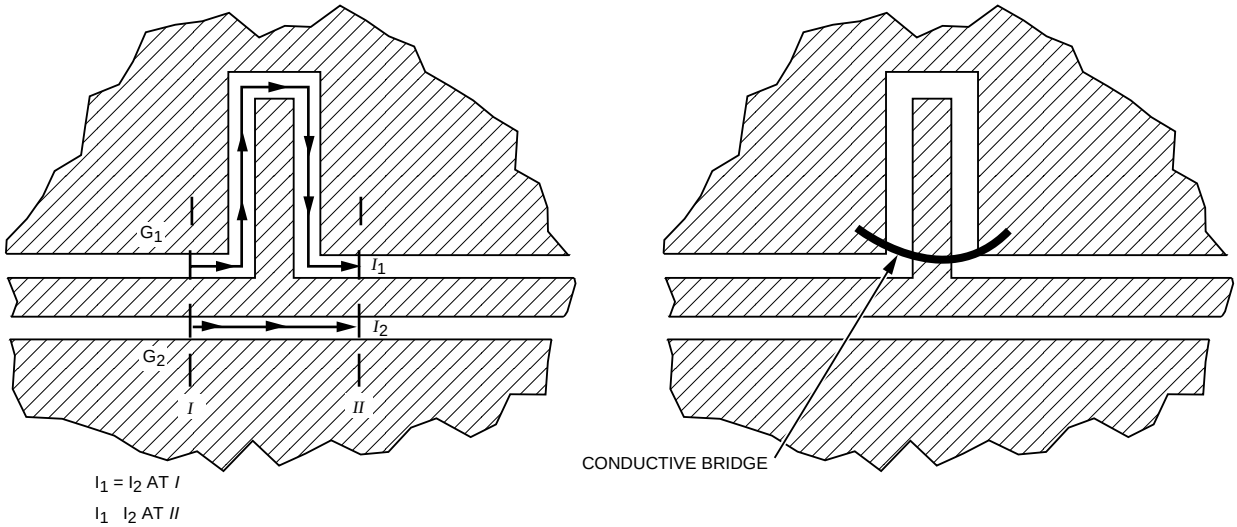


Figure 17. Control of Ground Currents in CPW.

conductor, extending into G2 as well as G1, the impedance would be slightly higher. Renewed interest in CPW has led to more studies of CPW discontinuities and models for them.[9]

Appendix B: HT-2 PCB Material

Several printed circuit board materials are in common use for RF circuits such as this one. Two of the most popular are FR4 and fiberglass reinforced PTFE (Teflon®). The former provides good mechanical stability and durability at low cost. However, it suffers from high losses and a dielectric constant which is poorly controlled and strongly frequency-dependent. The latter exhibits very good RF properties, but is expensive, suffers from poor mechanical stability, and cannot survive certain SMT (**S**urface **M**ount **T**echnology) processing steps. Hewlett-Packard's new **HT-2** board material provides durability and high temperature performance which are actually superior to FR4 with a controlled dielectric constant ($\varepsilon_r \cong 4.3$) and a loss tangent which is one third less than that of FR4. These properties make it ideal for microstrip circuits operating at frequencies up to or above 6 GHz.

To compare the performance of this material with FR-4 in a CPW, two experimental 50 Ω lines, 3.6 inches in length, were fabricated and tested. Cross section dimensions were identical in both cases, with board thickness = 0.032", linewidth = 0.043" and gapwidth = 0.006". Insertion loss and return loss were measured from 10 MHz to 8 GHz, using the same E.F. Johnson connectors described in the body of this paper. When the losses due to connector mismatch were subtracted, the resulting curve of resistive loss vs. frequency was linear in both cases. Using a value of $\varepsilon_{eff} = 2.70$ for the FR-4 and 2.57 for the **HT-2**, the loss vs. frequency curve was found to correspond to constant values of loss per wavelength. For the **HT-2** line, that constant was 0.5 dB/λ, much less than the 0.8 dB/λ of the FR-4 line. It is interesting to note that similar measurements on microstrip lines with h = 0.032" have resulted in identical values of loss/wavelength, even though the higher value of ε_{eff} on microstrip results in wavelengths which are shorter than those in CPW.

At the time of this printing HT-2 is available through Dan Schutte of International Circuits, 1319 S. Arkle St., Visalia, CA.

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